An Optimized Dual Active Bridge Converter for EV On-board Charger

Liu, Bochen

Publication date:
2020

Document Version
Publisher's PDF, also known as Version of record

AN OPTIMIZED DUAL ACTIVE BRIDGE CONVERTER FOR EV ON-BOARD CHARGER

BY
BOCHEN LIU

DISSERTATION SUBMITTED 2020

AALBORG UNIVERSITY
DENMARK

An Optimized Dual Active Bridge Converter for EV On-board Charger

Ph.D. Dissertation

Bochen Liu

Dissertation submitted Sep. 14, 2020

Dissertation submitted: Sep. 14, 2020

PhD supervisor: Professor Frede Blaabjerg
Aalborg University, Denmark

Assistant PhD supervisor: Associate Professor Pooya Davari
Aalborg University, Denmark

PhD committee: Associate Professor Daniel Ioan Stroe (chairman)
Aalborg University, Denmark

Associate Professor Junichi Itoh
Nagaoka University of Technology, Japan

Professor Omar Hegazy
Vrije Universiteit Brussel, Belgium

PhD Series: Faculty of Engineering and Science, Aalborg University

Department: Department of Energy Technology

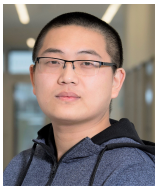
ISSN (online): 2446-1636
ISBN (online): 978-87-7210-807-0

Published by:
Aalborg University Press
Kroghstræde 3
DK – 9220 Aalborg Ø
Phone: +45 99407140
aauf@forlag.aau.dk
forlag.aau.dk

Printed in Denmark by Rosendahls, 2020

Curriculum Vitae

Bochen Liu



Bochen Liu received the B.Sc. and M.Sc. degree in Electrical Engineering from Southeast University, China, in 2014 and 2017, respectively. In association with his graduations, he received the honors of Excellent Undergraduate Student and Outstanding Postgraduate Student. He was a visiting student researcher at the University of Cambridge during the period from March 2020 to August 2020, working in the research group led by Dr. Teng Long. His main research interests include modeling and control of the grid-connected converters and the application of power electronics and relevant reliability analysis in electric vehicles.

Curriculum Vitae

Abstract

With the global interests and efforts to popularize electric vehicles (EVs) due to their zero carbon emission, the EV sales are increasing fast in recent years. As key part, the on-board charger (OBC) considerably facilitates the development of the EV industry by providing the freedom to fueling the vehicle anywhere electricity is available, especially in the metropolitan areas. However, due to the space and weight limitation in an EV, the OBC requires a high power density DC-DC converter transferring the power from a rectified DC-link to the battery pack in the vehicle. The dual active bridge (DAB) converter has drawn worldwide attention as a promising candidate for the OBC application. Much research has been done to improve the DAB performance regarding different aspects such as efficiency and reliability. Nonetheless, there are still challenges ahead, which should be addressed to advance the on-board charging.

Firstly, an accurate modeling of the DAB converter is needed to investigate the effect of the control variable on the power transfer. Due to the high-frequency ac current of the transformer, it is challenging to build an accurate DAB model because the commonly used moving average model is no longer suitable. Besides, the model is expected to incorporate the power dissipation on the active and passive components so that it can offer an easy way to evaluate the whole OBC performance and alleviate the controller design.

Secondly, one key advantage of the DAB converter is the zero-voltage-switching (ZVS) achievement for all power semiconductor devices. However, the ZVS is easy to lose in light load and can not be guaranteed in a wide battery voltage range. The soft-switching failure could lead to greatly increased switching losses due to the high switching frequency, and even further destroy the power device caused by excessive changing rate of the drain-source voltage during the switching transients. Therefore, accurate ZVS range calculation is demanded for the DAB design.

Thirdly, the DAB converter has larger conduction losses compared to other topology counterparts. Many optimization methods have been proposed in literature to suppress the conduction losses. However, the close-loop control procedure would become more complex if employing the improved

method. Hence a simple and easy optimization scheme is needed in respect to an easy real-time control.

Fourthly, the ambient temperature could be very high under the vehicle hood. This will challenge the reliable operation of the DAB converter by overheating the pivotal components such as the power semiconductor device. Therefore, during the usage phase of the OBC, an active thermal management method is needed to achieve higher system reliability.

Aiming to tackle these challenges, this Ph.D project investigates the corresponding solutions. The high frequency ac current in the DAB converter is modeled by considering individual harmonic components. The modeling procedure and mathematical derivation are analyzed in detail. It turns out that different harmonic components dominate the modeling accuracy depending on the loading situations. Then the soft-switching conditions are derived based on the practical switching transition. The key point is to include the non-linear output capacitance of the power device into the ZVS calculation. In order to validate the soft-switching conditions, a comprehensive comparison with the prior-art calculation methods are implemented.

Next, a linear control strategy is presented to reduce the conduction losses without sacrificing the other converter performances. The DAB converter is operated with two modulation schemes for different power loading. The operating principle behind this hybrid modulation is explained from the original loss distribution to the final linear control derivation. Finally, the conventional driving signal with a fixed 50% duty cycle is modified to regulate the loss distribution. As a result, the thermal stress of the power devices can be controlled and redistributed. Operating the DAB converter in various loading situations, the measured case temperatures in the experiments are able to demonstrate the effectiveness of the modified modulation scheme.

Resumé

EV-salget steget betydeligt i de senere år, som følge af globale interesser og bestræbelser på at popularisere elektriske køretøjer (EV'er), på grund af deres nul kulstofemission. En vigtig del er den indbyggede oplader, som påvirker udviklingen af EV-industrien betydeligt ved at give frihed til at tanke køretøjet hvorend elektricitet er tilgængelig, som især gør sig gældende i storbyområderne. Samtidigt kræver en indbygget oplader en DC-DC-konverter med høj effekttæthed, som overfører strømmen fra en ensrettet DC-link til batteripakken i køretøjet, på grund af plads- og vægtbegrænsning i et elektrisk køretøj. Den dobbelte aktive bro (DAB) konverter har fået verdensomspændende opmærksomhed ifm. at være en lovende kandidat til realisering af den indbygget lader. Der er udført en betydelig mængde forskning med formålet at forbedre DAB-ydeevnen med hensyn til forskellige aspekter såsom effektivitet og pålidelighed. Der er dog stadig udfordringer, som bør løses for at fremme indbygget opladning.

For det første er der brug for en nøjagtig modellering af DAB-konverteren for at undersøge effekten af kontrolvariablen som dikterer effektoverførslen. Som følge af transformer vekselstrømmens højre frekvens, er det udfordrende at opbygge en nøjagtig DAB-model, da den almindeligt anvendte gennemsnitsmodel ikke længere er egnet. Desuden forventes det, at modellen indeholder effekttabet af de aktive og passive komponenter, så den kan evaluere ydelsen af den indbygget lader og dermed gøre regulator designet nemmere.

Desuden er en af nøglefordelene ved DAB-konverteren, dens evne til at levere nul-spændings tilstandsændring for alle halvleder enheder. Evnen til at levere nul-spændings tilstandsændring kan dog ikke garanteres under let last, hvilket gør sig gældende i et større batterispændings område. Den manglende evne til at levere nul-spændings tilstandsændring kan føre til en kraftig forøgelse ændringstab på grund af den høje ændringsfrekvens og kan i værste fald endda skade halvlederkomponenten som følge af overdreven ændring af dens blokeringsspænding under de transiente forløb ved tilstandsændring. Det er dermed yderst vigtigt at bestemme hvilket område det er muligt at realisere nul-spændings tilstandsændring.

Ydermere har DAB-konverteren større ledningstab sammenlignet med

andre topologier. Der er blevet foreslået mange optimeringsmetoder for at mindske ledningstabet i gældende litteratur, disse metoder gør dog lukketsløjfe reguleringen mere kompleks og der er derfor et behov for en simpel optimeringsmetode med hensyn til at opnå enkel realtidsregulering.

Derudover kan temperatur blive høj under køretøjets motorhjelm og dette kan udfordre den pålidelige drift af DAB-konverteren som følge af en overophedning af de centrale komponenter såsom halvlederen. Derfor er der under brugsfasen af den indbygget lader behov for en aktiv termisk reguleringsmetode for at opnå højere systempålidelighed.

Med henblik på at overkomme disse udfordringer undersøger dette ph.d.-projekt mulige løsninger. Den højfrekvente vekselstrøm i DAB-konverteren er modelleret ved at tage de individuelle harmoniske komponenter under overvejelse. Modelleringens proceduren og de matematiske afledninger er analyseret med en stor mængde detalje. Det viser sig at de forskellige harmoniske komponenter har større indflydelse på modelleringsnøjagtigheden afhængigt af laststilstanden. Derefter er nul-spændings tilstandsændrings forholdene afledt på basis af den praktiske tilstandsovergang. Den afgørende faktor er at inkludere den ikke-lineære udgangskapacitans af enheden under beregning af nul-spændings tilstandsændring. Med henblik på at validere betingelser for nul-spændings tilstandsændringen, er en omfattende sammenligning med de kendte beregningsmetoder implementeret.

Efterfølgende præsenteres en lineær reguleringsstrategi med henblik på at reducere ledningstab uden at ofre konverterens øvrige præstationer. DAB-konverteren opereres ved brug af to moduleringsordninger under forskellige effektbelastninger. Operationsprincippet bag denne hybridmodulation er forklaret ud fra tabsfordeling og den endelige lineære regulerings udledning. Endelig er det konventionelle operatingssignal der er baseret på en fast driftscyklus på 50% ændret for at ændre tabsfordeling. Dermed kan effektenhedernes termiske stress kontrolleres og derved omfordel es. I forbindelse med eksperimentelle forsøg opereres DAB-konvertere under forskellige lasttilstande, hvorved enhedens kassetemperaturer måles, hvilket kan demonstrere effektiviteten af den modificerede moduleringsordning.

Contents

Preface

The work presented in this dissertation is a summary of the outcome from the Ph.D project "*An Optimized Dual Active Bridge Converter for EV On-board Charger*", which was carried out at the Department of Energy Technology, Aalborg University, Denmark. This PhD project is supported by China Scholarship Council, Department of Energy Technology, Aalborg University, Otto Mønsteds Fond, University of Cambridge, and Innovation Fund Denmark through the Reliable Power Electronic based Power System (REPEPS) project. The author would like to give an acknowledgment to the above-mentioned institutions.

First of all, I would like to express my sincere gratitude to my supervisor Professor Frede Blaabjerg for his consistent support and patient guidance during the running of this project. I would not have made it through my Ph.D research without his valuable feedback and overall insights. I would also like to express my deep appreciation for my co-supervisor Associate Professor Pooya Davari for his dedicated guidance and help during the entire period of the Ph.D project. It has been such an inspiring experience to work under his supervision.

I am also grateful to Doctor Teng Long for offering an opportunity to visit University of Cambridge during my study abroad. I would also like to thank my colleagues at University of Cambridge for their great hospitality during my stay.

Special thanks go to Associate Professor Yongheng Yang and Assistant Professor Dao Zhou for their valuable suggestions and help. I would also like to thank all my colleagues and secretaries at the Department of Energy Technology, Aalborg University for their support and fruitful discussion.

Last but not least, I would like to express my gratitude to my family for their endless care and continued encouragement, which is the greatest support in many ways.

Bochen Liu
Aalborg University, Sep. 14, 2020

Report

Chapter 1

Introduction

1.1 Background

1.1.1 Electric Mobility Transition

The depleting reserve of fossil energy and increasing concern for the environment is driving the transportation industry towards electrification [1]. Instead of using gasoline or diesel as energy source in the conventional internal combustion engine (ICE) vehicles, the emerging competitive counterparts, electric vehicles (EVs), are directly driven by the eletricity power from an on-board energy storage (e.g. battery pack or supercapacitors). According to whether the vehicles are partially or fully driven by the electricity, there are hybrid electric vehicles (HEVs) and battery electric vehicles (BEVs). The EVs will be more eco-friendly because the battery packs can be charged from sustainable sources of electricity like solar or wind [2–7], especially as the global penetration level of renewable energy is increasing at a very fast rate annually. Besides, the problem of noise pollution in cities can also be solved if EVs can fully replace the ICE vehicles. Many automobile manufacturers are participating in this mobility transition by developing and commercializing their own electric models, and over 7 million EVs are on the roads now [1]. Considering that the sale of EVs is still less than 0.5 million before 2013, the EVs will account for a lot more in the transportation industry in the future and it is expected that over 250 million will haven been sold by 2030 [1].

However, in order to accomplish this anticipated changeover from ICE vehicles to EVs in the near future, there are two main goals that need to be achieved: **a)** a technical breakthrough to increase the battery capacity and **b)** the development of suitable and preferable on-board battery chargers. The low battery capacity directly limits the driving range on a fully charged battery (also known as range anxiety), which is usually between 100 km and

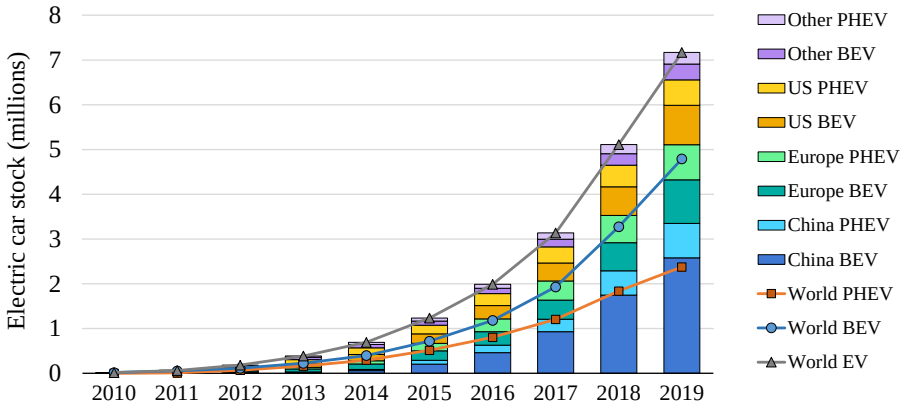


Fig. 1.1: Global electric vehicle stock including plug-in hybrid electric vehicles (PHEVs) and battery electric vehicles (BEVs), 2010 - 2019 [1].

Table 1.1: International Charging Standards for Different Power Levels

Plug	**Charging Level**	**AC/DC Voltage, Current, Maximum Power**
SAE J1772	AC Level 1	1Φ, 120 Vac, $\leq$ 12 A, 1.44 kW 1Φ, 120 Vac, $\leq$ 16 A, 1.9 kW
	AC Level 2	1Φ, 208 - 240 Vac, $\leq$ 80 A, 19.2 kW
IEC 62196	Type 1	1Φ, 230 Vac, 10 - 16 A, 3.68 kW
	Type 2	1Φ, 230 Vac, 16 - 32 A, 7.4 kW
	Type 3	3Φ, 400 Vac, $\leq$ 32 A, 22 kW
CHAdeMO	DC Level 3	200 - 500 Vdc, $\leq$ 400 A, 200 kW
SAE, CCS, Combo	DC Level 3	200 - 1000 Vdc, $\leq$ 350 A, 350 kW
Tesla US	DC Level 3	Model S, 400 Vdc, $\leq$ 300 A, 120 kW

500 km for a modern EV. As comparison, most gasoline cars have an average range of 500 km and the diesel cars even have a larger range of 800 km. Therefore, most EV manufacturers have been competing fiercely on the energy storage technique. The other concern limiting the spread of EV is the longer refueling time (30 minutes $\sim$ 10 hours or more) compared to ICE vehicles (5 $\sim$ 10 minutes or less). Hence, the battery charger should be continuously upgraded to satisfy the advancing battery capacity and the requirement of fast charging.

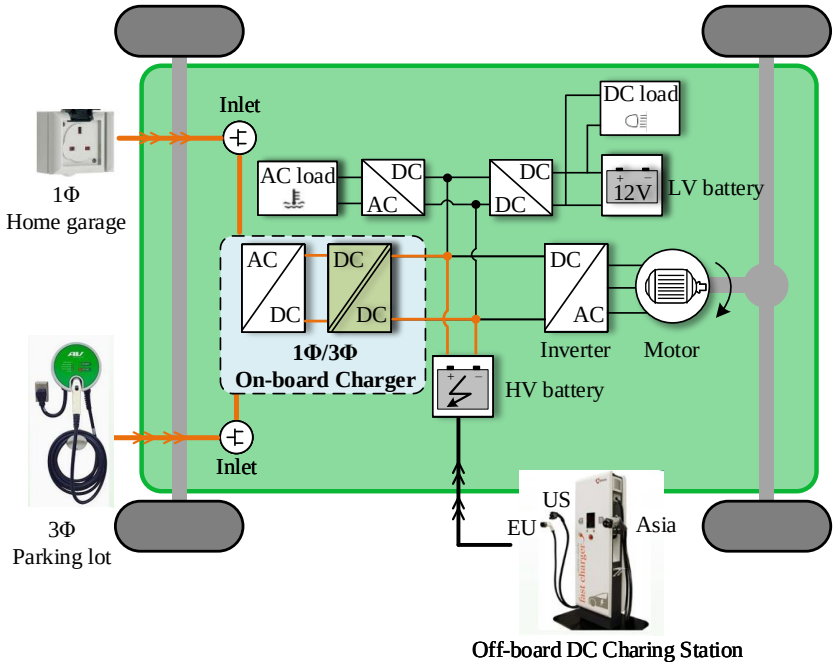


Fig. 1.2: Power electronic system structure in an EV.

Generally, there are two ways to charge an EV: **a) off-board charging** and **b) on-board charging** [8], both of which are depicted in Fig. 1.2. At present, the main charging standards and relevant charging levels around the world are summarized in Table 1.1. Similar to a gas station used for ICE vehicles, an off-board DC charging station can fast/ultra-fast charge the battery up to 80% of full capacity within 15 minutes or less. However, the charging stations are not popularized yet at all as the gas stations and this is only necessary when people are undergoing a long journey driving. Regarding the on-board charger (OBC), it can liberate the consumers from the need of searching for charging stations and allow them to charge their vehicles from almost any single-phase or three-phase power socket, as long as the charging instruments (mainly the charging cables and connectors) can withstand the required charging power (3.3 kW $\sim$ 22 kW). Therefore, this project considers the on-board charging application.

According to whether the drivetrain propulsion power electronic components are utilized during the charging process, the on-board chargers can be categorized into **a) integrated** and **b) standalone** types. The integrated chargers [8, 10–15] usually use a combination of the drivetrain inverter and the windings of the propulsion motor for EV charging, and hence realize

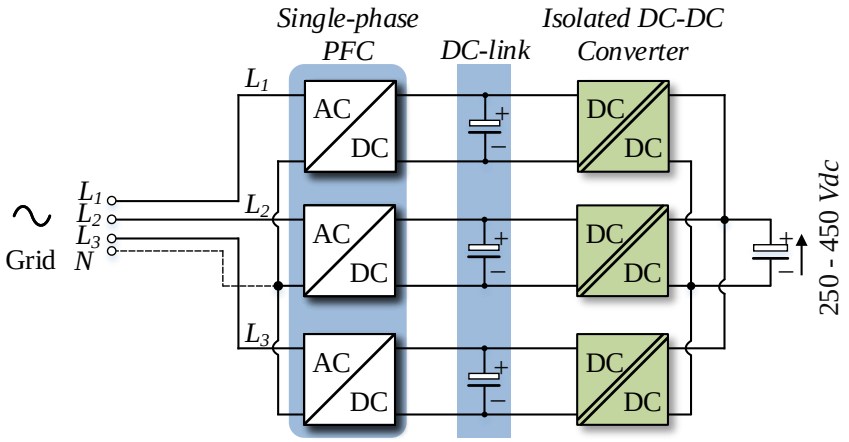


Fig. 1.3: Block diagram of three-phase OBC for Tesla Model 3 [9].

AC to DC power conversion and AC current filtering. This integrated type can mitigate the space and weight restrictions of the battery charger on an EV and raise the charging power level up to 50 kW. A commercialized example is the integrated 'Chameleon' charger in Renault Zoe having a rated power of 43 kW. However, this straightforward integration could generate unwanted torque in the machine as the AC currents flow through the motor windings. Due to this, the motor has to be mechanically locked, which might cause a long-term damage to the rotation shaft and gear box and thus decrease the machine lifetime. In addition, the propulsion motor and associated drives need to be redesigned (e.g. multiphase structure) because the popularized three-phase machine cannot be fully and conveniently integrated into the charging process [16]. Another concern is that classical induction motor driving system adopts non-isolated inverter topologies, offering no isolation between the mains and the traction battery. This conflicts with safety standards if the battery is connected to the car chassis [11, 17].

In terms of the standalone OBCs, most of them are designed with a power between 6.6 kW and 7.4 kW for now and with 3.3 kW in the early stage. The power level is mainly determined by the available main grid voltage and the rated current of the charging connector. Single-phase OBC is currently the most adopted charger in market with a maximum 19.2 kW (cf. Table 1.1) according to [18]. However, it is more often to adopt three-phase charging if the power is above 7.4 kW considering the efficiency and component counts. The main limitation of standalone OBC is the weight and space constraints in an EV. Hence, the single- and three-phase charging are often integrated in one circuit. For example, the three-phase OBC of Tesla Model 3 is composed of three single-phase charging modules in order to compromise with both

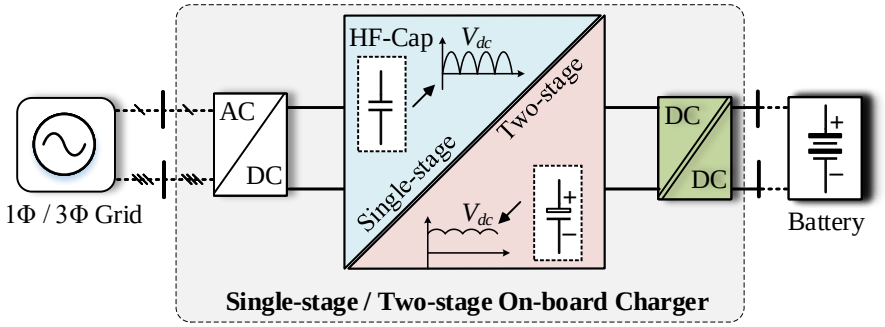


Fig. 1.4: A simplified charging structure of the single-stage and two-stage OBCs.

single-phase and three-phase charging connectors [9], which is as shown in Fig. 1.3. Besides, thanks to the development of semiconductor technology, the size limitation now can be substantially alleviated by using wide-band-gap SiC or GaN power devices [19]. This allows for higher switching frequency, and the resultant lower energy storage requirement in each switching cycle helps to shrink the size of magnetic and capacitive components in the OBC. As a result, it is shown in [20] that the power density can be approximately doubled if the switching frequency is increased by a factor of ten. Due to this, this Ph.D project investigates the power electronics in standalone on-board charger.

1.1.2 On-board Charging Systems

According to whether a DC-link is involved in the charging system, the available on-board chargers (OBCs) can be classified into **a) two-stage** and **b) single-stage** types.

In the commonly used two-stage OBCs, the DC-link capacitor is usually interfaced as the energy storage element to decouple the front-end AC-DC stage and the rear-end DC-DC stage, which can be found in Fig. 1.4. Due to this, flexible converter choices for the AC-DC and DC-DC conversion stages becomes possible in order to satisfy various charging requirements, such as modular design to unify the different charging standards.

Regarding the single-stage OBCs [21, 22], the motivation is to remove the DC-link electrolytic capacitor (E-cap) bank from the charging system. This could benefit the charger size and converter lifetime. There are mainly two single-stage circuit structures: one is using a matrix converter to transfer the line-frequency current to the high-frequency ac current of the transformer [23–25], and the other is replacing the electrolytic capacitor with a high-frequency (HF) filtering capacitor (cf. Fig. 1.4) [26] . For both structures,

complex control scheme has to be adopted in order to accomplish power factor correction (PFC) and achieve an acceptable converter efficiency. In detail, the grid voltage is usually assumed constant during one switching period in the single-stage charger. This is reasonable because of a much higher switching frequency compared to the line frequency. The power devices have to switch fast to suppress the grid current harmonics and meanwhile keep the fundamental component in phase with the grid voltage. Hence only with high switching frequency, the single-stage charger can guarantee a high power factor. On this basis, soft-switching technique becomes a necessary part of the control in order to offset the efficiency deterioration and thermal stress increment caused by high switching frequency. This will further complicate the control process because the soft-switching range should be wide enough to enclose the grid voltage. Considering the concerns above, the two-stage structure is still the favored option by most EV manufacturers, with the advantages of convenient control, wide line regulation and high power factor.

As shown in Fig. 1.4, the two-stage OBC comprises AC-DC and DC-DC conversions interconnected by DC-link capacitor. Regarding the conversion from ac line voltage to DC-link voltage, there are four popular topologies, i.e. boost power factor correction (PFC) converter [8], totem-pole bridgeless PFC converter [19, 27–29] and single-/three-phase bridge based PFC converter [8]. The PFC converter is necessary to reduce the grid-connected current harmonics for fulfilling specific charging standards and should be designed with high efficiency to maximize the power flowing to the downstream DC-DC converter.

The (interleaved) boost PFC converter is currently the most commercialized rectifier due to its advantages of simple design, reliable operation, fast system control loop and low cost. However, the disadvantages are also obvious such as low power factor, bulk passive components and significant power losses caused by the diode bridge. In addition, the poor performance of the reverse recovery in Si super junction semiconductors could lead to addition power losses as well as severe oscillations and voltage spikes. With the emerging of wide-band-gap (WBG) power devices, the trend of PFC converter design is moving towards the bridgeless structure (e.g. totem-pole PFC) and the utilization of WBG devices. Thus, the power losses are considerably reduced in the conduction path, and WBG devices become the ideal candidate because of their superior properties in terms of very low or even eliminated reverse recovery, decreased on-state resistance and high voltage capability. The research of AC-DC conversion will not be included in this Ph.D project because of the mature technology on rectifier design. Therefore, as the output of AC-DC conversion, the DC-link will be simulated by a constant DC voltage, which is the input of the following isolated DC-DC conversion stage.

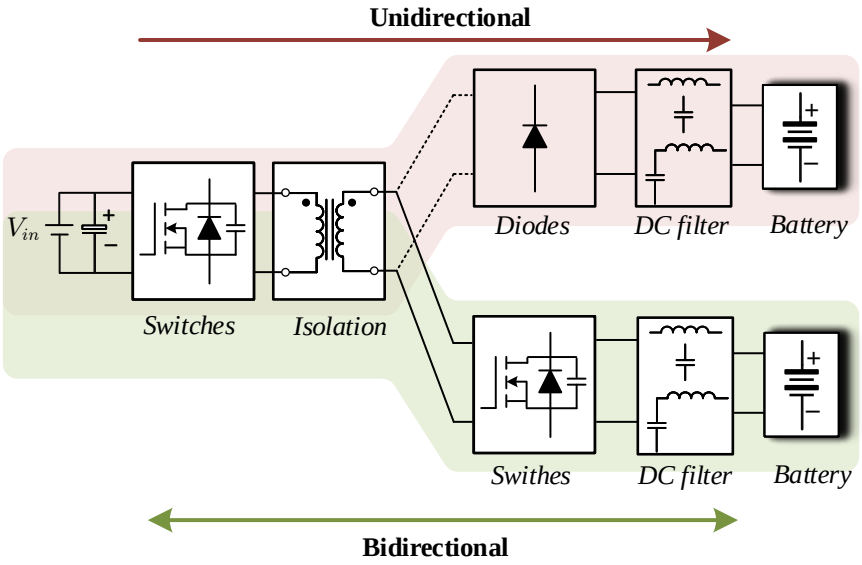


Fig. 1.5: Block diagram of unidirectional and bidirectional isolated DC-DC converters for OBCs.

With regards to the DC-DC conversion stage, it can be seen from Fig. 1.4 that this stage is decoupled with the front-end AC-DC stage by a DC-link in the standalone type of OBC. Considering the safety issues from the customer side, a high-frequency transformer is often adopted to isolate battery with the DC-link. Hence, compared to AC-DC conversion, the DC-DC stage usually comprises more components including power semiconductors and other passive components. Besides, since the battery pack is directly paralleled on the output DC port, more complex control and careful power regulation should be considered in the DC-DC conversion, together with much higher switching frequency than the AC-DC conversion. Therefore, the DC-DC converter will be the focus of this Ph.D thesis by assuming the input DC voltage is constant. The utilized DC-DC converter for OBCs can be either unidirectional or bidirectional. As shown in Fig. 1.5, the power flow directions and corresponding circuit structures are different for unidirectional and bidirectional isolated DC-DC converters.

Currently, unidirectional DC-DC converters are most widely employed and one typical topology is the phase-shift full-bridge converter featuring of electrical isolation and diode bridge on the battery side. However, from a long-term perspective, bidirectional DC-DC converter will be the trend by supporting energy feeding from the battery back to the grid. This is known as the concept of vehicle to grid [30–34]. Besides, the bidirectional architecture also can save much power loss from the diode bridge. Due to reasons above,

the bidirectional isolated DC-DC converter structure is considered for the DC-DC conversion in an OBC.

Focusing on the bidirectional isolated DC-DC conversion (cf. Fig. 1.5), there are mainly four circuit configurations that are widely employed in the OBC application, i.e. **a) the bidirectional phase-shift full-bridge (PSFB) converter** [35] , **b) the LLC resonant converter** [36–38], **c) the three-phase dual-active-bridge (DAB) converter** [39] and **d) the dual-active-bridge converter** [40]. Their circuit topologies are shown in Fig. 1.6.

As shown in Fig. 1.6(a), the bidirectional PSFB converter is a derivative of the conventional PSFB converter where the secondary side of the transformer is a diode bridge. With proper modulation, the high-voltage side power devices $Q_1 \sim Q_4$ can achieve zero-voltage-switching (ZVS) and the low-voltage side $Q_5 \sim Q_8$ zero-current-switching (ZCS). However, this converter can only reduce voltage from V_{in} to nV_{out} due to that the duty cycle of the primary voltage v_p is typically used to control the power transfer. Besides, special modulation scheme is needed in order to achieve the reverse power flow from V_{out} to nV_{in}.

Regarding the bidirectional LLC converter in Fig. 1.6(b), it can achieve a slightly higher efficiency than the DAB converter with reduced transformer current and switching losses. However, larger magnetic components (i.e. the transformer and inductor) are needed to provide sufficient energy storage, and an additional resonant capacitor is necessary. Hence, an EV should leave more space for the OBC if the LLC converter is utilized.

A shown in Fig. 1.6(c), the three-phase DAB converter can achieve the lowest voltage and current stress for the transformer and power devices among the four topologies. However, this configuration needs a large number of circuit components including transformers, inductors and switches, which is not cost-effective and requires a higher volume for EV. Besides, the efficiency performance is not as good as the LLC and DAB converters according to [41].

With respect to the DAB converter in Fig. 1.6(d), it only has one inductor and is highly flexible in terms of the modulation scheme and the symmetric circuit structure. The main challenges for applying DAB converter are the higher transformer RMS current, and the complex modulation algorithm to properly drive the power devices. From the perspective of smaller size and lower component counts, the DAB converter for the OBC application is selected as the target topology in this Ph.D project.

1.2 Project Motivation

In order to regulate the power transfer of the DAB converter, phase-shift modulation scheme is often applied. The principle is generating a phase shift

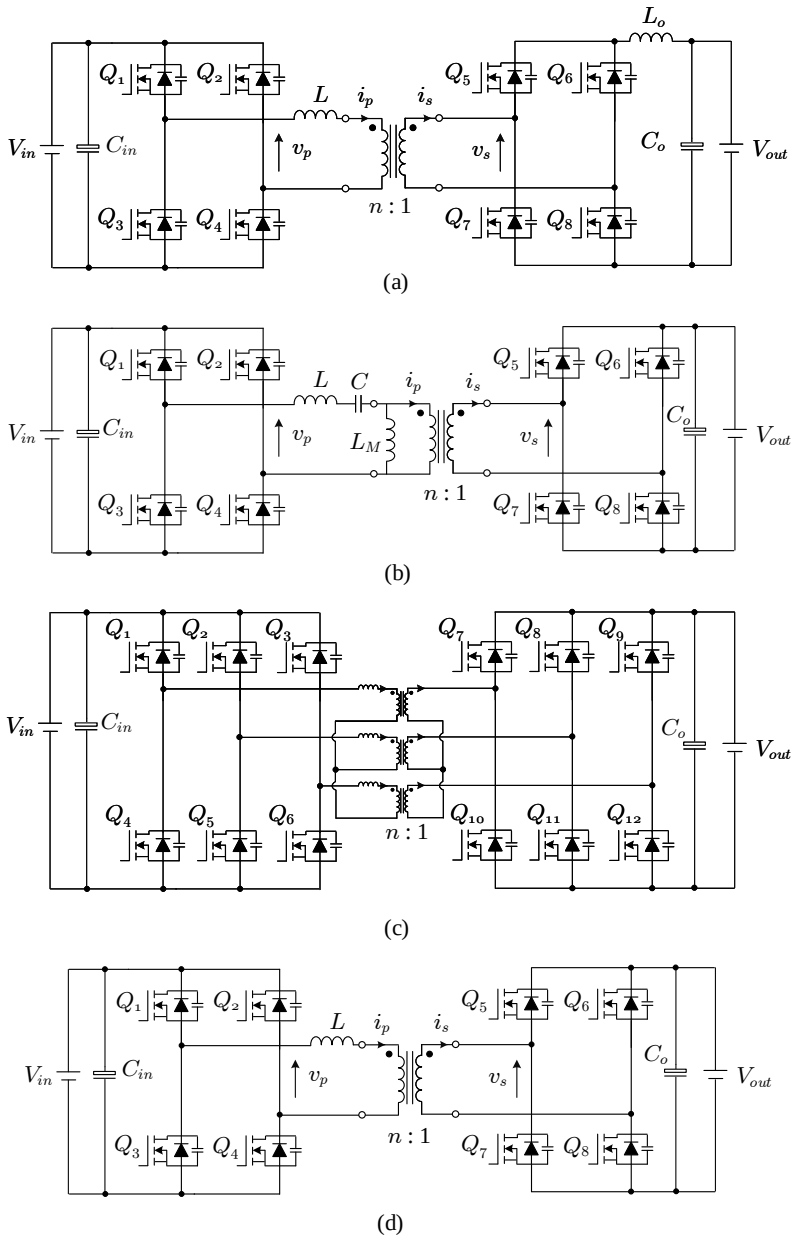


Fig. 1.6: Popular bidirectional isolated DC-DC converters for battery charging application: (a) Phase-shift full bridge converter (b) LLC resonant converter (c) Three-phase dual-active-bridge converter (d) Dual-active-bridge converter

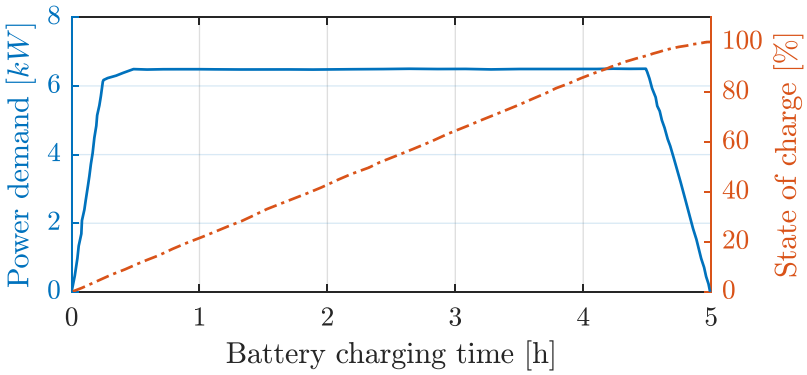


Fig. 1.7: Charging profile of Nissan LEAF battery pack [43].

between the primary and secondary full-bridge terminal voltages, as denoted by v_p and v_s in Fig. 1.6(d). There is usually a stringent limitation on the phase shift in order to suppress the induced reactive power [42]. This means that the expected power transfer range of the DAB converter is limited by the varying range of the controlled phase shift. A practical charging profile of the Nissan LEAF battery is shown in Fig. 1.7. Considering a fact that the charging power in an OBC usually varies widely, e.g. from zero to 6.6 kW in Fig. 1.7, a challenge is induced in mapping the restricted control variable range with the wide power transfer range.

Zero voltage switching (ZVS) is an essential characteristic of the DAB converter in order to achieve the high efficiency and high power density. Therefore, apart from the limited phase shift range by the power regulation, the control variable is also limited by the ZVS realization. The ZVS range is fixed for a given DAB converter with the constant input and output dc voltages. However, the battery voltage in an OBC is not constant during the charging process and it usually varies in the range of 250 V $\sim$ 450 V for EVs. For instance, the voltage profile of a single battery cell is shown in Fig. 1.8. As a result, the ZVS range varies with the battery voltage, which induces a challenge of operating the DAB converter within the changing ZVS range throughout the whole charging process.

With the phase shift modulation scheme, this phase shift will inevitably cause a circulating current in the circuit and generate a higher power loss than other counterpart topologies. In order to further improve the DAB converter efficiency, the power loss should be reduced without compromising other converter performances such as the power transfer range and ZVS. In other words, the control variables need accurate regulation to fulfill the three conditions of power transfer requirement, ZVS achievement and loss reduction. This will be a big challenge for an easy real-time control with varying

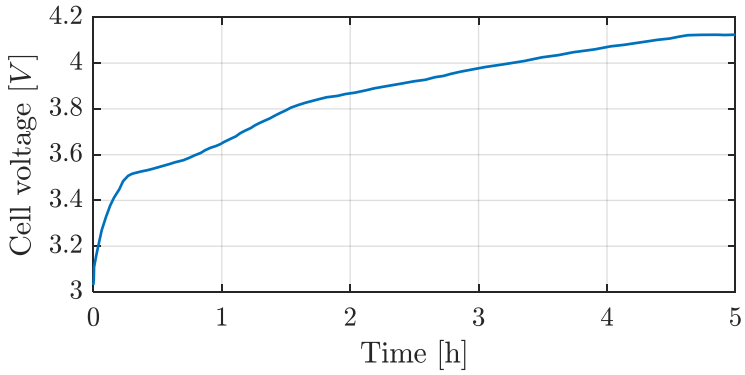


Fig. 1.8: Lithium-ion battery cell voltage during the charging process [44].

power demand and battery voltage during the charging process.

Inside an EV, the on-board charger usually share one cooling system with the drivetrain and the motor engine for the sake of cost and complexity [45], hence the coolant temperature could be as high as $100^{\circ}C$. In addition, the outside ambient air temperature under the hood could reach $50^{\circ}C$ in the worst case scenario [46]. The resultant overtemperature might lead to the melting of large-area soldering between the adjacent layers in a power semiconductor. Besides, this high temperature could greatly affect the material reliability such as the power substrate, power die attachment and encapsulation [47]. As the most vulnerable components, the reliability of the power semiconductor in a DAB converter confronts the challenge of the high ambient temperature.

According to the challenges discussed above, the main motivation and project tasks of this Ph.D. project for developing an optimized DAB converter for the OBC application is shown in Fig. 1.9.

1.3 Research Questions and Objectives

The final goal of this Ph.D project is to develop a high efficiency and high reliability DAB converter for the OBC application. Considering the challenges discussed above, the main research question is: how to properly manipulate the control variables for achieving a wide ZVS range, minimum power loss and enhanced thermal management in the DAB converter? Accordingly, there is the project hypothesis: an accurate DAB model, the precise ZVS boundary calculation, a simplified real-time control scheme and the active thermal control can facilitate solving the proposed question. In detail, the main question can be divided into four sub-questions in the following.

- What is the relationship between the control variable and the control

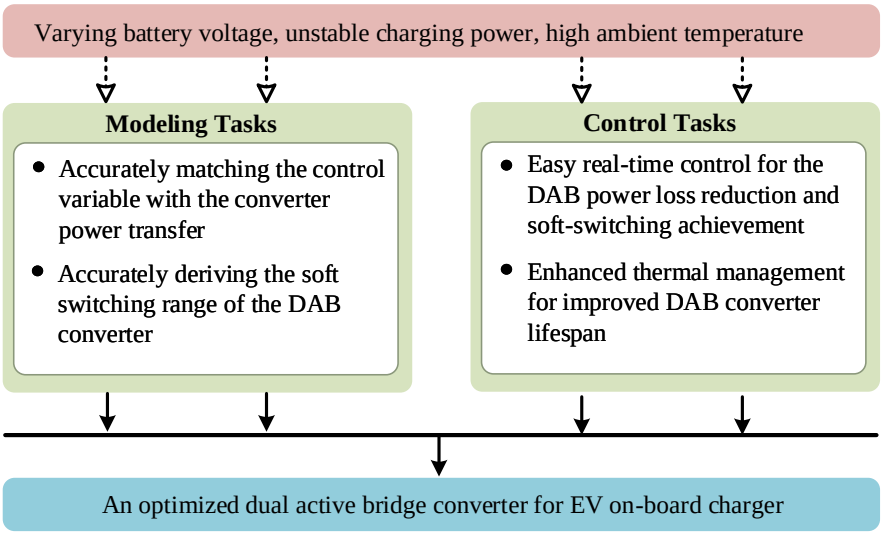


Fig. 1.9: Research tasks of this Ph.D thesis.

target ?

- How to calculate the ZVS range with varying battery voltages and charging powers ?
- Is it possible to simplify the complex modulation scheme and meanwhile reduce the conduction losses?
- Is it possible to manage the thermal distribution in a DAB converter to improve its adaption to the harsh environment on EV ?

According to the research questions above, the project objectives are summarized as:

- **Develop an enhanced DAB model which can accurately describe the connection between the phase shift and power transfer**

  Generally, an ideal DAB model is used to determine the varying range of the controlled phase shift for a specific power transfer requirement from light load to rating load. The phase shift should be controlled in a proper range such that it can guarantee a wide power range and achieve a relatively low reactive power transmission. Besides, the ideal active and passive components are often assumed in the design phase in order to calculate the maximum transfer power. This ideal assumption will result in a relatively low accuracy and adversely affect the component

selection and transformer design in the beginning. In the OBC application, the battery is usually connected with the DAB converter at one dc port, and hence the widely varying charging power and battery voltage would require a precise control to make fully use of the limited phase shift range. Therefore, an accurate DAB model is needed.

- **Derive a calculation method which can accurately identify the ZVS range when the DAB converter is operated with varying dc voltages and power levels**

  The DAB converter can naturally achieve ZVS for all power devices if the control variables are properly regulated. This advantage can facilitate the usage of DAB converter in high power density application, including the on-board EV charger. There are two drawbacks considering the OBC application. Firstly, the DAB converter is prone to lose the soft-switching ability in light loading situations. Secondly, during the closed-loop control procedure, a saturation is often used to limit the control parameters within ZVS range. The upper and lower limitation values should be changed accordingly along with the battery voltage and required charging power. Otherwise, the converter would operate beyond the ZVS range and the regulation ability on the transfer power will be degraded. In either case, the resultant ZVS failure could lead to large switching losses and even totally break the power device because of excessive dv/dt. Thus, the ZVS boundary should be accurately identified in widely different operating situations.

- **Develop a simple control scheme to handle the complex control procedure with the capability of losses optimization**

  There are mainly two targets concerning the control variables regulation: one is fulfilling the required power transfer and the other is guaranteeing the DAB converter to operate in ZVS range. The multiple phase shift control technique is commonly utilized to realize these targets, which will complicate the real-time control procedure. Besides, massive mathematical calculations are required to derive the optimal operating points in terms of losses reduction. Furthermore, the computational burden might become larger as the ZVS range saturation changes on-line with the feedback of the varying battery voltage. In order to enable an easy control and a higher efficiency, a fast real-time control scheme is needed.

- **Develop a method of active thermal management without sacrificing other converter performances**

  In most of the reliability research, it is assumed that the failure of one component causes the whole system failure. In a DAB converter, the

power devices could have different parameters (e.g. on-state resistance) due to the manufacturing tolerances. This will cause different thermal stress on the power devices although they might switch simultaneously. Moreover, the imperfect circuit design (e.g. asymmetric current flowing path) could further enlarge this thermal unbalance. Consequently, the power rating and lifetime of the DAB converter are limited by the most stressed device. Therefore, an active thermal management is needed for improving the system reliability.

1.4 Project Limitations

The following hypotheses, simplifications and limitations have been performed in this Ph.D project.

- This Ph.D project focus on the DC-DC stage of an OBC and the DAB converter is picked out to realize the power transfer from the DC-link to the battery loading. There are several hypotheses and limitations considering a comprehensive study of the OBC for EVs. The AC-DC conversion from single-phase or three-phase grid AC input to the DC-link output is also an important part of the OBC, which is closely related to the grid-connection power quality and energy exchange between the battery and the grid. This AC-DC stage is not researched in this project. As shown in Fig. 1.4, the input voltage of the DC-DC stage is actually the DC-link voltage in a two-stage OBC, but it is assumed to be a constant DC voltage in this work.
- An EMI filter is usually interfaced between the grid and the rectifier in practice in order to fulfill the EMI standards for the OBC. This is essential for the EV application since many micro electronics components are assembled and they can be easily affected by the EMI. From the perspective of high power density, the EMI filter usually occupies one third of the total volume and weight of an OBC. If the EMI filter can be optimized with the minimum size, the power density of the OBC can be considerably improved. The EMI filter is not considered in this project.
- In an EV, the charging power is usually controlled by the battery management system (BMS). In this project, the DAB converter power is directly given.
- The actual charging power levels and voltage levels are listed in Table 1.1. In this project, a scale-down experimental DAB converter prototype is built to validate the modeling and control methods.

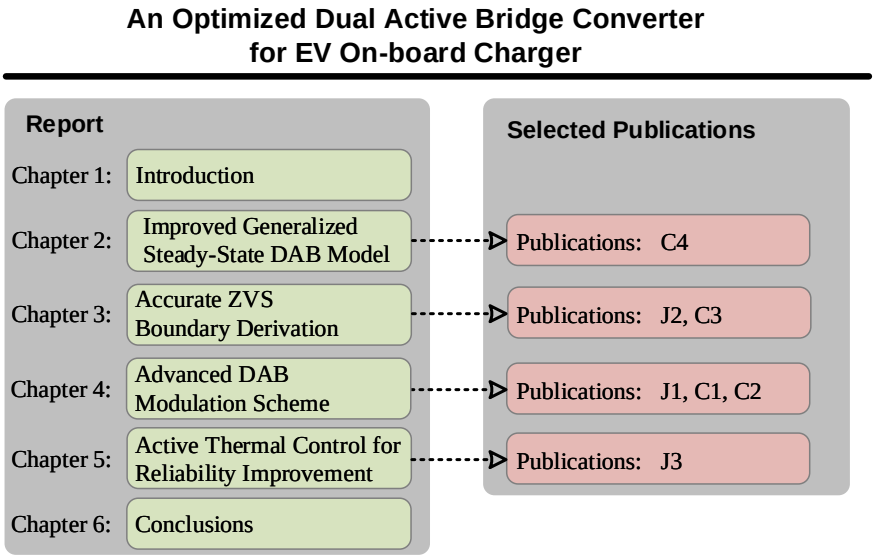


Fig. 1.10: Thesis structure with related topics and research outcomes for each chapter.

1.5 Thesis Outline

The outcomes of the Ph.D project are documented in the Ph.D thesis, mainly comprised of two parts: report and selected publications. The report gives a summary of the research conducted during the Ph.D study, and partial research outcomes are reflected in the selected publications. The thesis frame is as shown in Fig. 1.10, providing a guideline of linking the report with selected publications.

The report part is organized into six chapters. In Chapter 1, an introduction of the project background and research objectives is given. Then focusing on the DC-DC conversion stage in an on-board charger, the subsequent four chapters tackle research challenges with the DAB converter from different perspectives. Chapter 2 derives an accurate DAB model considering a practical converter prototype. The modeling methodology and deriving procedure are elaborated and further validated by the experiments. In Chapter 3, based on the measured practical switching transients, an accurate calculation method to define the ZVS range is introduced. A comprehensive comparison among the prior-art calculation methods is implemented. Together with the proposed approach, they are fully evaluated and validated with various system configurations. The main focus of Chapter 4 is on the trade-off between the converter requirement and the optimization objective. On this basis, a simplified control strategy is formulated and applied to the

built setup for a practical validation. Chapter 5 mainly focuses on the active thermal management of the DAB converter. Considering the unbalanced thermal loading of the power semiconductor devices, a modified modulation scheme is proposed to suppress this unbalance and further improve the converter reliability. Finally, the last chapter summarizes the main contribution of this Ph.D project and outlines the future research perspectives.

1.6 List of Publications

The research outcomes during the Ph.D. study are in forms of journal papers and conference publications, as listed in the following. And parts of them are used in the Ph.D. thesis as in Fig. 1.10.

Journal Papers

J1. **B. Liu**, P. Davari and F. Blaabjerg, "An Optimized Hybrid Modulation Scheme for Reducing Conduction Losses in Dual Active Bridge Converters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, DOI: 10.1109/JESTPE.2019.2956323, 2019.

J2. **B. Liu**, P. Davari and F. Blaabjerg, "Nonlinear Coss-VDS Profile based ZVS Range Calculation for Dual Active Bridge Converters," *IEEE Trans. Power Electron.*, DOI: 10.1109/TPEL.2020.3003248, 2020.

J3. **B. Liu**, P. Davari and F. Blaabjerg, "A Hybrid Modulation Scheme for an Enhanced Thermal Management of Dual Active Bridge Converters," *IEEE Trans. Power Electron.*, in preparation, 2020.

- F. Blaabjerg, H. Wang, I. Vernica, **B. Liu** and P. Davari, "Reliability of Power Electronic Systems for EV/HEV Applications," *Proceedings of the IEEE*, under review, 2020.

Conference Papers

C1. **B. Liu**, P. Davari and F. Blaabjerg, "An Optimized Control Scheme for Reducing Conduction and Switching Losses in Dual Active Bridge Converters," in *Proc. IEEE ECCE* , Sept. 2018, pp. 622-629.

C2. **B. Liu**, P. Davari and F. Blaabjerg, "An Optimized Control Scheme to Reduce the Backflow Power and Peak Current in Dual Active Bridge Converters," in *Proc. IEEE APEC*, Mar. 2019, pp. 1622-1628.

C3. **B. Liu**, P. Davari and F. Blaabjerg, "Enhanced Zero-Voltage-Switching Conditions of Dual Active Bridge Converter Under Light Load Situations," in *Proc. IEEE APEC*, Mar. 2020, DOI: 10.1109/APEC39645.2020.9124213.

C4. **B. Liu**, P. Davari and F. Blaabjerg, "An Enhanced Generalized Average Modeling of Dual Active Bridge Converters," in *Proc. IEEE APEC*, Mar. 2020, DOI: 10.1109/APEC39645.2020.9124001.

- **B. Liu**, P. Davari and F. Blaabjerg, "A Flexible Control Scheme for Single-Stage DAB AC/DC Converters," in *Proc. IEEE PEAC* , Nov. 2018, pp. 1-6.

- Z. Chen, **B. Liu**, P. Davari, and H. Wang, "Efficiency Enhancement of Bridgeless Buck-Boost PFC Converter with Unity PF and DC Split to Reduce Voltage Stresses," in *Proc. IEEE IECON*, Oct. 2018, pp. 1187–1192.
- Z. Shen, Y. Shen, **B. Liu** and H. Wang, "Thermal Coupling and Network Modeling for Planar Transformers," in *Proc. IEEE ECCE*, Sept. 2018, pp. 3527–3533.

Book chapter

- **B. Liu**, D. Zhou and F. Blaabjerg, "*Advanced Modeling and Control of VSCs with LCL Filters*," in Control of Power Electronic Converters and Systems, 3rd ed., Frede Blaabjerg, Ed.: Elsevier, 2020, ch. 8.

Chapter 2

Improved Generalized Steady-State DAB Model

2.1 Background

Many discrete-time models [48–51] of the DAB converter can be used to describe the converter states. In the OBC application, the battery voltage varies in a wide range ($250\ V \sim 450\ V$). Considering this, the relationship between the phase-shift angle and the output dc voltage of a DAB converter needs to be accurately modeled in order to provide proper reference for the design phase of an OBC. On this basis, a continuous-time model is necessary to accurately map the control variable to the power transfer.

The moving average technique [52] is extensively used to model the dc-dc converters, which requires that the state variable (e.g. inductance current or capacitor voltage) can be approximately replaced with an averaged dc variable. In other words, the ripple current/voltage should be small enough compared to the dc component so that it can be neglected. However, this assumption is not applicable to the DAB converter because of the high-frequency alternating current on both sides of the isolated transformer.

Considering that the periodic ac variable can be modeled by a complex Fourier series, the generalized average modeling (GAM) technique [53] is proposed to study the harmonic components of an ac variable and the cross-coupling of different harmonic components. By applying the GAM to the DAB converter, the prior-art research [54], [55] mainly focus on the small-signal modeling and frequency response. Of course, other modeling methods besides GAM can also be utilized to study the converter performance from different perspectives, such as the derived time-domain analytical expressions in [56], [57] and the discrete-time models [48], [50], [51], [58].

In some of the previous work, the DAB converter is regarded as an ideal converter without any power losses, or only partial losses are taken into account such as the conduction losses. This will lead to a non-negligible steady-state error. In addition, the first harmonic approximation (FAM) is often employed to derive the

DAB model in order to maintain a good tradeoff between the accuracy and complexity. However, this approximation might not be true over the whole power range and could lead to considerable steady-state errors (cf. Section 2.4). With respect to the time-domain analytical expression, massive calculations are needed in order to solve the steady-state equations corresponding to the piecewise sub-intervals of the leakage inductance current. This will result in a large computational burden. Furthermore, if the losses are taken into account, the piecewise linear approximation of the leakage inductance current will become piecewise exponential, which will dramatically increase the modeling complexity.

In order to accurately predict the steady-state response, an enhanced 1^{st}-order generalized average model of the DAB converter is firstly presented in this chapter. In this model, power losses caused by the power devices, the isolating transformer and the dc-link capacitor are taken into account. Besides, in order to analyze the effect of different harmonic components on the steady-state error, a universal generalized average model including 1^{st}-order up to h^{th}-order ($h = 1,\ 3,\ 5...$) harmonic components is derived. The importance of 3^{rd}-order harmonic component is highlighted when the converter is operated in light-load situations. Finally, experiments are conducted to validate the theoretical analysis.

2.2 Lossless Model

The commonly used DAB model without considering any power loss is shown in Fig. 2.1(a). V_{in} is the input DC voltage, and v_p, v_s are the high-frequency ac voltages generated by FB_1 and FB_2 on the primary and secondary side of the transformer, respectively. i_L is the primary leakage inductance current. i_o and v_o are the output dc current and voltage for the resistive load R_{load}. By applying the phase-shift modulation to the DAB converter, the working waveforms are as shown in Fig. 2.1(b), where φ is the control variable and denotes the phase shift between v_p and v_s. Noting that the diagonal power devices in one full-bridge (e.g. Q_1, Q_4 in FB_1) share the same driving signal and are switched with a fixed 50% duty cycle.

By introducing two switching functions $u_1(t)$ and $u_2(t)$

$$\begin{aligned} u_1(t) &= \begin{cases} 1, t \in [t_0, t_2] \rightarrow Q_1, Q_4 \text{ on} \\ -1, t \in [t_2, t_4] \rightarrow Q_2, Q_3 \text{ on} \end{cases} \\ u_2(t) &= \begin{cases} 1, t \in [t_1, t_3] \rightarrow Q_5, Q_8 \text{ on} \\ -1, t \in [t_0, t_1) \cup (t_3, t_4] \rightarrow Q_6, Q_7 \text{ on} \end{cases} \end{aligned} \tag{2.1}$$

to FB_1 and FB_2, respectively, the voltages v_p and v_s can be expressed by

$$\begin{cases} v_p(t) = u_1(t) \cdot V_{in} \\ v_s(t) = u_2(t) \cdot v_o(t) \end{cases} \tag{2.2}$$

Then the lossless switched model of the DAB converter shown in Fig. 2.1(a) can be

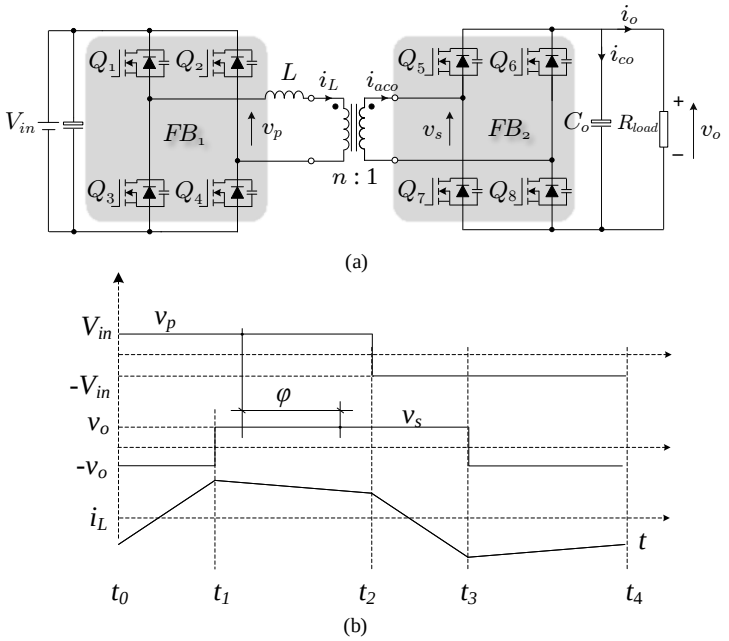


Fig. 2.1: DAB model and its operation: (a) Lossless DAB model with a resistive load (b) Operating waveforms with phase-shift modulation. [C4]

derived as

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}u_1(t)\cdot V_{in} - \dfrac{n}{L}u_2(t)\cdot v_o(t) \\ \dfrac{dv_o(t)}{dt} = \dfrac{n}{C_o}u_2(t)\cdot i_L(t) - \dfrac{1}{R_{load}C_o}v_o(t) \end{cases} \tag{2.3}$$

In the generalized averaged model (GAM) technique, a periodic signal $x(t)$ can be expressed as

$$x(t) = \sum_{k=-\infty}^{+\infty} \langle x\rangle_k(t)\cdot e^{jk\omega t} \tag{2.4}$$

where ω is the fundamental pulsation (e.g. the grid line frequency or switching frequency) and $\langle x\rangle_k(t)$ is the coefficient of the k^{th} harmonic, which is equal to

$$\langle x\rangle_k(t) = \frac{1}{T}\int_{t-T}^{t} x(\tau)\cdot e^{-jk\omega\tau}d\tau \tag{2.5}$$

with $T = 2\pi/\omega$. Deriving from (2.4) and (2.5), two fundamental properties [53], [59] of GAM can be obtained with

$$\begin{cases} \dfrac{d}{dt}\langle x\rangle_k(t) = \left\langle \dfrac{d}{dt}x\right\rangle_k(t) - jk\omega\langle x\rangle_k(t) \\ \langle x\cdot y\rangle_k(t) = \displaystyle\sum_i \langle x\rangle_{k-i}(t)\cdot\langle y\rangle_i(t) \end{cases} \tag{2.6}$$

For the convenience of derivation, $i_L(t)$, $v_o(t)$, $u_1(t)$, $u_2(t)$ in (2.3) are simplified with i_L, v_o, u_1, u_2, respectively. According to the first harmonic approximation (FHA) technique, the 1^{st}-order component of the ac current i_L and the 0th-order of the output DC voltage v_o are considered. On this basis, the generalized averaged model of the lossless DAB converter can be derived using (2.4) $\sim$ (2.6), resulting in

$$\begin{cases} \dfrac{d\langle i_L\rangle_1}{dt} = -j\omega\langle i_L\rangle_1 + \dfrac{1}{L}\langle u_1\rangle_1 \cdot V_{in} - \dfrac{n}{L}\langle u_2 \cdot v_o\rangle_1 \\ \dfrac{d\langle v_o\rangle_0}{dt} = \dfrac{n}{C_o}\langle u_2 \cdot i_L\rangle_0 - \dfrac{1}{R_{load}C_o}\langle v_o\rangle_0 \end{cases} \tag{2.7}$$

where $\omega = 2\pi f_{sw}$ and f_{sw} is the switching frequency.

The average values of the switching functions are usually equal to zero in order to avoid transformer saturation, i.e. $\langle u_1\rangle_0 = \langle u_2\rangle_0 = 0$. Therefore, according to [53], [59], there are

$$\begin{cases} \langle u_2 \cdot v_o\rangle_1 = \langle u_2\rangle_1 \cdot \langle v_o\rangle_0 \\ \langle u_2 \cdot i_L\rangle_0 = \langle u_2\rangle_1 \cdot \langle i_L\rangle_{-1} + \langle u_2\rangle_{-1} \cdot \langle i_L\rangle_1 \end{cases} \tag{2.8}$$

Therein, combining with (2.1), the 1^{st}-order harmonic component of $u_1(t)$ and $u_2(t)$ can be derived as

$$\langle u_1\rangle_1 = \frac{2}{j\pi}, \quad \langle u_2\rangle_1 = \frac{2}{j\pi} \cdot e^{-j\varphi} \tag{2.9}$$

On the other hand, according to (2.5), the real part (denoted by "R") and the imaginary part (denoted by "I") of an arbitrary k^{th}-order harmonic coefficient can be mapped to that of the $-k^{th}$-order harmonic coefficient, which are given as

$$\begin{cases} \langle x\rangle_{kR} = \dfrac{1}{T}\int_{t-T}^{T} x(\tau)cos(k\omega\tau)d\tau = \langle x\rangle_{-kR} \\ \langle x\rangle_{kI} = \dfrac{1}{T}\int_{t-T}^{T} x(\tau)sin(k\omega\tau)d\tau = -\langle x\rangle_{-kI} \end{cases} \tag{2.10}$$

Applying (2.8) $\sim$ (2.10) to the original lossless model (2.7), the DAB model can be expressed in a state-space form.

$$\frac{d}{dt}\begin{bmatrix}\langle i_L\rangle_{1R}\\ \langle i_L\rangle_{1I}\\ \langle v_o\rangle_0\end{bmatrix} = \begin{bmatrix}0\\ -\dfrac{2}{\pi L}\\ 0\end{bmatrix} V_{in} + \begin{bmatrix}0 & \omega & \dfrac{2n}{\pi L}sin\varphi\\ -\omega & 0 & \dfrac{2n}{\pi L}cos\varphi\\ -\dfrac{4n}{\pi C_o}sin\varphi & -\dfrac{4n}{\pi C_o}cos\varphi & -\dfrac{1}{R_{load}C_o}\end{bmatrix}\begin{bmatrix}\langle i_L\rangle_{1R}\\ \langle i_L\rangle_{1I}\\ \langle v_o\rangle_0\end{bmatrix} \tag{2.11}$$

2.3 Lossy Model of DAB converter

The commonly used lossless model in Fig. 2.1(a) is actually an ideal assumption of the practical DAB converter. It can be used as a rough approximated model in the converter design, such as the value of the leakage inductance. However, in the EV on-board charger application, the battery voltage (i.e. v_o) varies in a wide range and it is often regulated by the charging power, which is further determined by the phase-shift

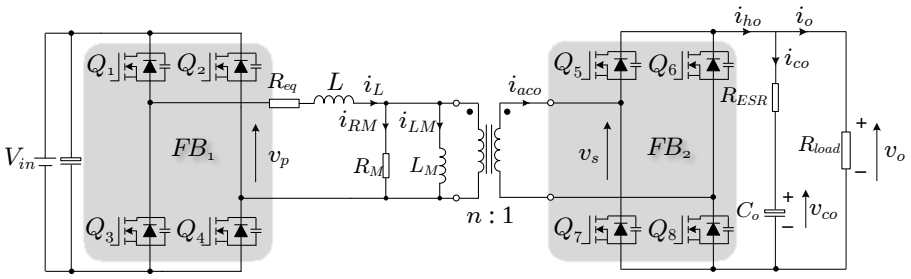


Fig. 2.2: A lossy DAB model considering conduction losses, core losses and the capacitor ESR losses. [C4]

φ in Fig. 2.1(b). Besides, the value of φ is also closely related to the soft switching realization. A small change of φ could lead to failed soft switching (cf. Chapter. 3), and the resultant high dv/dt can impair the converter performance and even damage the power devices. Therefore, an accurate relationship between the phase-shift φ and the output voltage v_o is vital for the charging application.

In light of this, a lossy model as shown in Fig. 2.2 is built, taking into account the core losses (represented by R_M), the conduction losses (represented by R_{eq}) and the capacitor losses (represented by the equivalent series resistor R_{ESR}). Note that the internal resistance of the input dc capacitor is not included because the input dc voltage is supplied by a constant voltage source in real experiments. In Fig. 2.2, by referring circuit parameters to the primary side of the transformer, the equivalent resistor R_{eq} can be calculated by

$$R_{eq} = 2R_{DS,onP} + R_{ind} + R_{trp} + n^2 R_{trs} + n^2 R_{DS,onS} \tag{2.12}$$

Therein, $R_{DS,onP}$ and $R_{DS,onS}$ are the on-state resistance of the power device in the primary and secondary full bridge, respectively. R_{trp} and R_{trs} are the resistance of the primary winding and secondary winding of the transformer, respectively. R_{ind} is the resistance of the auxiliary inductor. The turns ratio of the transformer is $n:1$ from the primary to the secondary winding. In the built DAB setup, each switch of $Q_5 \sim Q_8$ in the secondary HB_2 consists of two parallel power devices in order to reduce the current stress. Thus, the referred secondary-side on-state resistance is $n^2 R_{DS,onS}$.

According to Fig. 2.2, the lossy switched model can be derived as (2.13), where L_M is the magnetic inductance, i_{LM} is the magnetic current, i_{RM} the resistive current, i_{ho} the output current of FB_2 and i_{co} the output capacitor current. Similarly, focusing on the 1^{st}-order harmonic components of i_L, i_{LM} and the 0^th-order components of v_{co} and v_o, the real part and imaginary part of each state variable can be separated. Then the lossy GAM model of the DAB converter can be obtained with (2.14). Note that due to the consideration of the capacitor ESR, the capacitor voltage v_{co} is not equal to the output voltage v_o, which is different from the lossless model. The modeling relationship between v_{co} and v_o can be represented by the last two expressions of (2.14). The defined coefficient C_{sys} is used to simplify the expression form and it is constant for a given DAB converter setup .

$$\begin{cases} \dfrac{di_{LM}}{dt} = \dfrac{n}{L_M} \cdot u_2 v_o \\ i_{RM} = \dfrac{n u_2 v_o}{R_M} \\ i_{ho} = n u_2 \cdot (i_L - i_{RM} - i_{LM}) \\ v_o = v_{co} + R_{ESR} \cdot C_o \dfrac{dv_{co}}{dt} \\ \dfrac{dv_{co}}{dt} = \dfrac{i_{ho}}{C_o} - \dfrac{v_o}{R_{load} C_o} \\ \dfrac{di_L}{dt} = -\dfrac{R_{eq}}{L} \cdot i_L + \dfrac{1}{L} \cdot u_1 V_{in} - \dfrac{n}{L} \cdot u_2 v_o \end{cases} \tag{2.13}$$

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} \langle i_L \rangle_{1R} \\ \langle i_L \rangle_{1I} \end{bmatrix} = \begin{bmatrix} -R_{eq}/L & \omega & \dfrac{2n}{\pi L} sin(\varphi) \\ -\omega & -R_{eq}/L & \dfrac{2n}{\pi L} cos(\varphi) \end{bmatrix} \times \begin{bmatrix} \langle i_L \rangle_{1R} \\ \langle i_L \rangle_{1I} \\ \langle v_o \rangle_0 \end{bmatrix} + \begin{bmatrix} 0 \\ -\dfrac{2}{\pi L} \end{bmatrix} V_{in} \\ \dfrac{d}{dt}\begin{bmatrix} \langle i_{LM} \rangle_{1R} \\ \langle i_{LM} \rangle_{1I} \end{bmatrix} = \begin{bmatrix} 0 & \omega & -\dfrac{2n}{\pi L_M} sin\varphi \\ -\omega & 0 & -\dfrac{2n}{\pi L_M} cos\varphi \end{bmatrix} \times \begin{bmatrix} \langle i_{LM} \rangle_{1R} \\ \langle i_{LM} \rangle_{1I} \\ \langle v_o \rangle_0 \end{bmatrix} \\ \langle v_o \rangle_0 = \langle v_{co} \rangle_0 + R_{ESR} \cdot C_o \dfrac{d}{dt} \langle v_{co} \rangle_0, \quad C_{sys} = \dfrac{R_M R_{load}}{(n^2 R_{ESR} + R_M) R_{load} + R_M R_{ESR}} \\ \dfrac{d}{dt} \langle v_{co} \rangle_0 = \dfrac{C_{sys}}{C_o} \left[\dfrac{-4n}{\pi} \cdot \left[\langle i_L \rangle_{1R} sin(\varphi) + \langle i_L \rangle_{1I} cos(\varphi) \right] + \right. \\ \qquad \left. \dfrac{4n}{\pi} \left(\langle i_{LM} \rangle_{1R} sin\varphi + \langle i_{LM} \rangle_{1I} cos\varphi \right) - \left(\dfrac{n^2}{R_M} + \dfrac{1}{R_{load}} \right) \langle v_{co} \rangle_0 \right] \end{cases} \tag{2.14}$$

2.4 3rd-Order Harmonic Effect of the Leakage Inductance Current

Seen from the derived lossless model in (2.11), the 1^{st}-order harmonic is utilized to represent the leakage inductance current because it is the fundamental component. However, this representation is proper on the condition that the fundamental 1^{st}-order harmonic is the dominating component and other harmonics can be neglected compared to the fundamental portion. If V_{p1}, V_{p3} are defined as the 1^{st}- and 3^{rd}-order harmonic amplitudes of the primary voltage v_p and V_{s1}, V_{s3} are defined for v_s, the

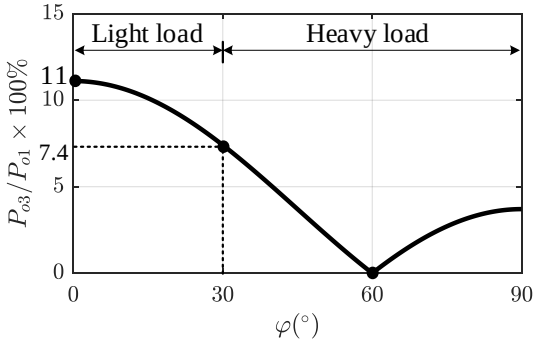


Fig. 2.3: The ratio of the 3^{rd}-order power component over the 1^{st}-order component. [C4]

power transfer of each harmonic component can be approximately calculated by

$$P_{o1} = V_{p1}V_{s1}\frac{sin\varphi}{\omega L}, \quad P_{o3} = V_{p3}V_{s3}\frac{|sin(3\varphi)|}{3\omega L} \tag{2.15}$$

where P_{o1}, P_{o3} denote the 1^{st}- and 3^{rd}-order harmonic power, and $\omega = 2\pi f_{sw}$ is the fundamental angular frequency.

Considering that $V_{p3} = 1/3V_{p1}$ and $V_{s3} = 1/3V_{s1}$, the ratio of P_{o3}/P_{o1} will be

$$\frac{P_{o3}}{P_{o1}} = \frac{sin(3\varphi)}{27 \cdot sin\varphi} \tag{2.16}$$

Based on (2.16), the characteristic of the power ratio P_{o3}/P_{o1} varying with the phase shift φ is depicted in Fig. 2.3. Since the transfer power increases with the phase-shift φ, the light-load region and heavy-load region are also shown in Fig. 2.3. It can be seen that the power ratio in the range of $\varphi > 60^\circ$ is relatively smaller, such as $P_{o3}/P_{o1} = 2\%$ for $\varphi = 70^\circ$. This small value indicates that the 1^{st}-order approximation of the leakage inductance current is proper with a large phase shift.

However, the power ratio dramatically increases in light load situations with a minimum value of 7.4% at $\varphi = 30^\circ$, and it becomes larger with the decrease of φ. If φ is low enough, the power ratio reaches the maximum 11% where $sin\varphi \approx \varphi$ and $sin(3\varphi) \approx 3\varphi$ are satisfied. In these situations, the 1^{st}-order approximation is not proper any more, and the 3^{rd}-order component should be considered for an accurate DAB model.

Without loss of generality, a universal GAM of the DAB converter is derived considering 1^{st}-order up to h^{th}-order ($h = 1,\ 3\ ,5...$) harmonic components, as expressed by (2.17). Similar to (2.14), the magnetic current (i_{LM}), the leakage inductance current (i_L), the capacitor voltage (v_{co}) and the output dc voltage (v_o) are selected as the state variables in (2.17). The first state-space equation in (2.17) denotes the real and imaginary parts of the k^{th} ($k = 1,3,5...h$) order harmonic component. In terms of the magnetic current modeling shown by the second state-space equation in (2.17), only the 1^{st}-order harmonic component is considered for i_{LM} since it is much smaller than i_L. Regarding the capacitor voltage and the output dc voltage, the averaged value

$$
\begin{cases}
\dfrac{d}{dt}\begin{bmatrix}\langle i_L\rangle_{kR}\\ \langle i_L\rangle_{kI}\end{bmatrix} = \begin{bmatrix} -R_{eq}/L & k\omega & \dfrac{2n}{k\pi L}sin(k\varphi) \\ -k\omega & -R_{eq}/L & \dfrac{2n}{k\pi L}cos(k\varphi)\end{bmatrix} \times \begin{bmatrix}\langle i_L\rangle_{kR}\\ \langle i_L\rangle_{kI}\\ \langle v_o\rangle_0\end{bmatrix} + \begin{bmatrix}0\\ -\dfrac{2}{k\pi L}\end{bmatrix} V_{in} \\
\dfrac{d}{dt}\begin{bmatrix}\langle i_{LM}\rangle_{1R}\\ \langle i_{LM}\rangle_{1I}\end{bmatrix} = \begin{bmatrix} 0 & \omega & -\dfrac{2n}{\pi L_M}sin\varphi \\ -\omega & 0 & -\dfrac{2n}{\pi L_M}cos\varphi\end{bmatrix} \times \begin{bmatrix}\langle i_{LM}\rangle_{1R}\\ \langle i_{LM}\rangle_{1I}\\ \langle v_o\rangle_0\end{bmatrix} \\
\langle v_o\rangle_0 = \langle v_{co}\rangle_0 + R_{ESR}\cdot C_o\dfrac{d}{dt}\langle v_{co}\rangle_0, \;\; C_{sys} = \dfrac{R_M R_{load}}{(n^2R_{ESR}+R_M)R_{load}+R_M R_{ESR}} \\
\dfrac{d}{dt}\langle v_{co}\rangle_0 = \dfrac{C_{sys}}{C_o}\left[\dfrac{-4n}{\pi}\sum_{k=1,3,5..}^{h}\dfrac{\langle i_L\rangle_{kR}sin(k\varphi)+\langle i_L\rangle_{kI}cos(k\varphi)}{k} + \right. \\
\left. \dfrac{4n}{\pi}\left(\langle i_{LM}\rangle_{1R}sin\varphi + \langle i_{LM}\rangle_{1I}cos\varphi\right) - \left(\dfrac{n^2}{R_M}+\dfrac{1}{R_{load}}\right)\langle v_{co}\rangle_0\right]
\end{cases}
\tag{2.17}
$$

Table 2.1: System Specifications of the Built DAB converter [C4]

Parameters	Description	Value
P	Rated power	1.5 kW
V_{in}	Input DC voltage	120 V
$n:1$	Turns ratio of the transformer	3.5 : 1
f_{sw}	Switching frequency	60 kHz
T_{dead}	Dead time	400 ns
L_{ind}	Auxiliary inductor	36.2 μH
L_{trp}	Primary-side leakage inductance	4.5 μH
L_{trs}	Secondary-side leakage inductance	372.5 nH

(i.e. 0^{th}-order component) is still the focus, as expressed by the last two equations in (2.17).

Table 2.2: Component Parameters of the Implemented Prototype [C4]

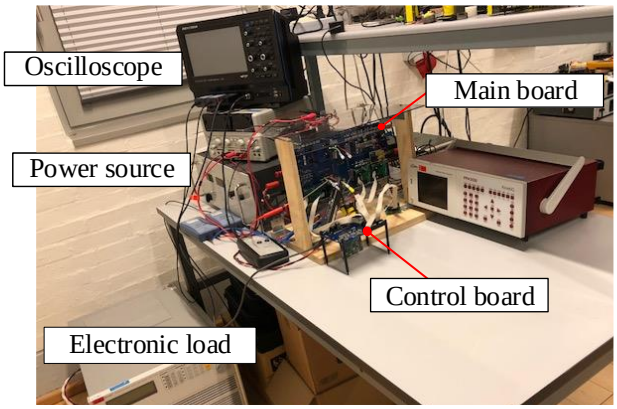
Components	Parameters
Auxiliary inductor: 10 turns Litz wire, 20 strands, strand diameter 0.355 mm	R_{ind}= 27.9 mΩ @T_a= 25 ^oC
Primary winding of the HF transformer: 35 turns copper foil	R_{trp}= 607.9 mΩ @T_a= 25 ^oC
Secondary winding of the HF transformer: 10 turns copper foil	R_{trs}= 16.5 mΩ @T_a= 25 ^oC
Magnetic inductance of the transformer	L_M = 1.4 mH
Core losses resistance	R_M= 2kΩ @T_a= 25 ^oC
MOSFETs $Q_1 \sim Q_4$: IPW65R080CFD	$R_{DS,onp}$= 72 mΩ @T_j= 25 ^oC
MOSFETs $Q_5 \sim Q_8$: 2 x IPP110N20N3 in parallel	$R_{DS,ons}$=9.6 mΩ @T_j= 25 ^oC
Resistive load	R_{load}= 2.3 Ω
Output capacitor C_o: 2 x EETEE2D301HJ in parallel	R_{ESR}= 30 mΩ @T_a= 25 ^oC

Table 2.3: Test Condition in Light Load and Heavy Load Situations

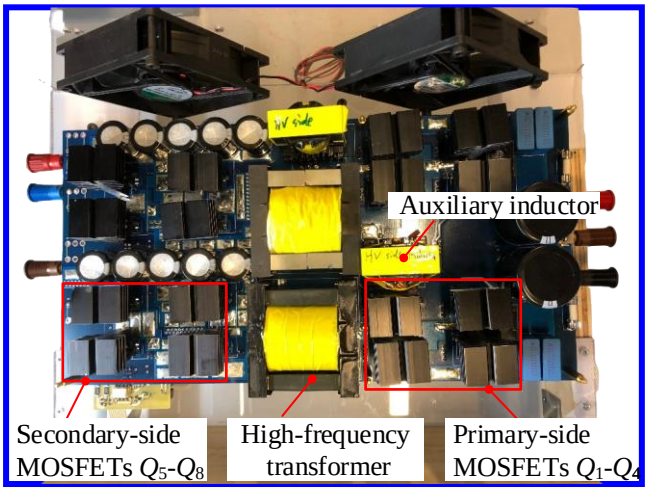
Parameters	Description	Light-load	Heavy-load
P_o	Output power	280 W	590 W
φ	Phase-shift angle	30^o	60^o
V_o	Output DC voltage	25 V	37 V
V_{in}	Input DC voltage	120 V	120 V
R_{load}	Resistive load	2.3 Ω	2.3 Ω

2.5 Experimental Validation

Given the DAB converter parameters listed in Table 2.1, a test platform is built as shown in Fig. 2.4. As denoted in Fig. 2.2, the total leakage inductance can be calculated by $L = L_{ind} + L_{trp} + n^2 L_{trs}$. The other circuit parameters associated with the



(a)



(b)

Fig. 2.4: Pictures of experimental setup. (a) test platform for the built DAB converter (b) top view of the main board of DAB. [C4]

lossy model Fig. 2.2 are measured and listed in Table 2.2.

Corresponding to the loading situations in Fig. 2.3, the DAB converter is switched between light-load and heavy-load situations by regulating the phase shift φ between 30° and 60°. The converter parameters under light-load and heavy-load test conditions are listed in Table 2.3. The dynamic response is illustrated in Fig. 2.5 where i_L is the primary leakage inductance current, v_p is the primary terminal voltage and v_o is the output dc voltage. The steady state working waveforms in two different load situations are shown in Fig. 2.6, corresponding to the gray areas in Fig. 2.5(a). The shape of the leakage inductance current is different depending on the output dc

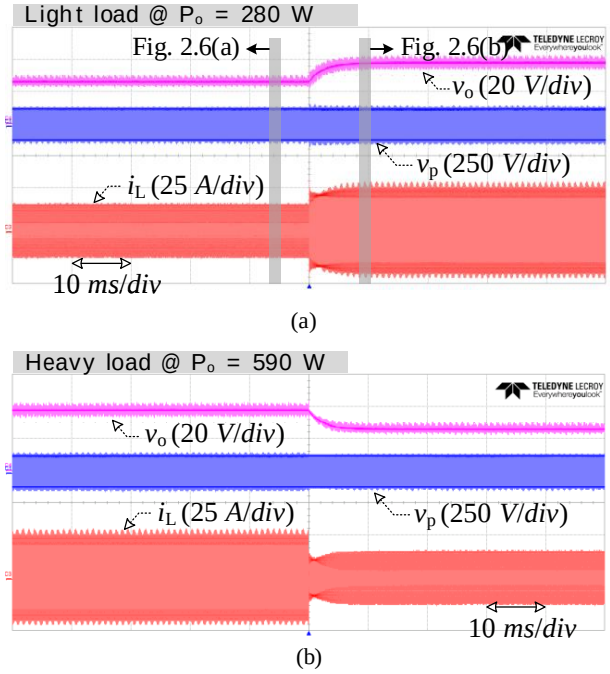


Fig. 2.5: Measured step response of the DAB converter: (a) with φ changing from 60° to 30° (b) with φ changing from 30° to 60°. [C4]

voltage, which is further controlled by the phase shift φ.

In order to fully evaluate the modeling accuracy of different generalized average models, the output dc voltage v_o is sampled by the oscilloscope and imported into MATLAB, as the gray waveforms shown in Fig. 2.7. By numerically averaging the actual v_o, the 0^{th}-order component of v_o can be obtained and shown by the black line in Fig. 2.7. As comparison, the modeled v_o waveforms using lossless GAM, 1^{st}-order GAM and 3^{rd}-order GAM are also shown in Fig. 2.7, as denoted by the solid red line, the solid blue line and the dashed red line. For a clear view, the v_o waveform within $t \in [-0.03s, -0.01s]$ and $t \in [0.02s, 0.04s]$ in Fig. 2.7(a) are amplified, as shown in Fig. 2.7(b) and Fig. 2.7(c), respectively.

Obviously, seen from Fig. 2.7(b) and Fig. 2.7(c), the lossless model will cause large error in both loading situations. In terms of the 1^{st}-order lossy model, it can considerably decrease the error in heavy load (cf. Fig. 2.7(c)). Nevertheless, in light load, the lossy model has a little effect on the error decrement in Fig. 2.7(b). Regarding the 3^{rd}-order lossy model, it can significantly reduce the errors between the modeling and experimental results in both loading situations. In other words, the 3^{rd}-order lossy model can improve the modeling accuracy over the whole power range, while the 1^{st}-order model is only effective in heavy loading situation, which is consistent with the previous theoretical analysis.

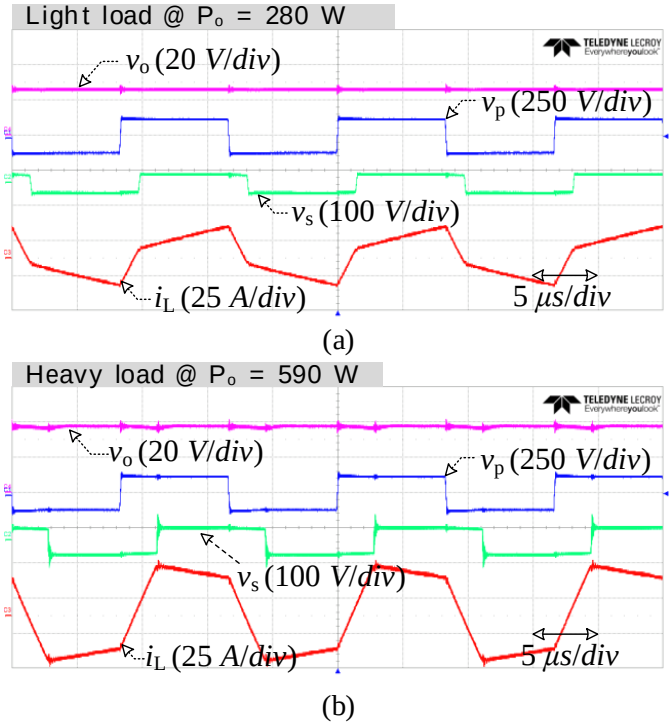


Fig. 2.6: Measure steady state operating waveforms of the DAB converter with (a) $\varphi = 30°$. (b) $\varphi = 60°$. [C4]

2.6 Summary

By taking into account the power losses in the modeling of the DAB converter, a universal lossy GAM of DAB is derived and the accuracy is effectively improved compared to the commonly used lossless model. Instead of only considering the 1^{st}-order fundamental component, the 3^{rd}-order harmonic component of the leakage inductance current is proposed and highlighted in this chapter, which can achieve a considerably improved modeling accuracy in light loading situations. The feasibility of the modeling accuracy and the 3^{rd}-order harmonic effect is validated with experimental results. By employing the derived 3^{rd}-order DAB lossy model in a wide power transfer range, the modeling accuracy of the DAB converter is improved compared to the conventional lossless model and 1^{st}-order model. According to the built model, the relationship between the control variable and the control target (e.g. load voltage, power transfer) can be accurately identified, which will benefit the zero-voltage-switching range derivation in Chapter 3 and the converter control in Chapter 4.

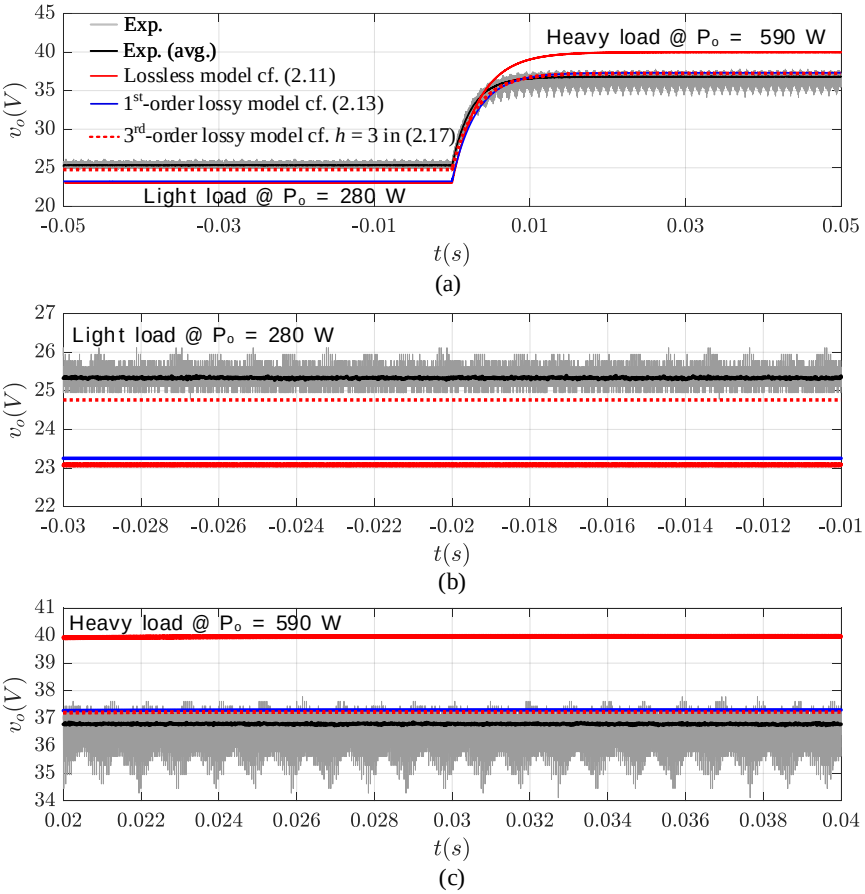


Fig. 2.7: Comparison of the modeling results with a step response (a) phase shift φ changed from 30° to 60° at $t = 0s$. (b) Zoomed-in waveforms for $t \in [-0.03s, -0.01s]$ in Fig. 2.7(a). (c) Zoomed-in waveforms for $t \in [0.02s, 0.04s]$ in Fig. 2.7(a). [C4]

Chapter 3

Accurate Zero-Voltage-Switching Boundary Derivation

3.1 Background

High power conversion efficiency is a principal merit of the DAB converter due to the inherent capability of zero-voltage-switching (ZVS) in all switches of this converter. However, the ZVS operation can be lost in light loads, especially if a high voltage ratio between the input port and the output port is required and the phase-shift modulation is used to regulate the power transmission. For the EV on-board charger (OBC) application, the input port of the DAB is usually associated with a high dc-link voltage (typical 400 V) and the output port is connected with the battery pack. Depending on the EV types, the output port voltage might vary in a wide range of 200 V $\sim$ 450 V. Besides, it is common that power electronic converters are usually designed to achieve the highest charging efficiency at rated power, whereas majority of the time they work in partial loading situations. This is also applicable to OBCs, whose daily load profiles are possibly within the light and medium load range in urban transportation usage. Furthermore, due to the fast developing of wide-band-gap (e.g. SiC and GaN) power devices in EVs, higher switching frequency becomes available and often adopted to shrink the size of passive components, benefiting the compact design of an OBC. Hence, it is imperative to guarantee soft switching in light-load operation of the DAB converter in order to avoid impairments caused by ZVS failure, such as increased switching losses, poor electromagnetic compatibility (EMC) performance [60] and even damaging power devices [61].

As shown in Fig. 3.1, there are three popular methods in literature to identify the ZVS boundary, namely current-, energy- and charge-based methods. The current-based method [62, 63] is derived according to the drain current direction when the transistor is turned on. In detail, the anti-parallel diode in a power device is con-

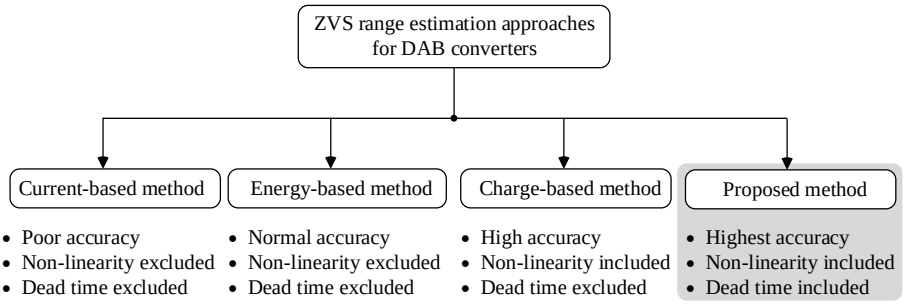


Fig. 3.1: Prior-art and proposed methods for estimating DAB zero-voltage-switching range.

ducted to provide a near-zero drain-source voltage for ZVS and thus the current direction is from source to drain. On this basis, the ZVS is regarded successful in the current-based method if the current direction is correct. However, this ZVS condition only considers the positive or negative direction of the drain current at the turn-on instant, which is not sufficient to guarantee a soft turn-on because the amplitude of the current also should be large enough. In the energy-based method [64], the calculation principle is that the energy stored in the output capacitance is totally released through the resonance between the output capacitance and the leakage inductance. Hence after the resonance, the power device can be softly turned on. This principle is legitimate and a minimum drain current can be derived accordingly. Nonetheless, the non-linear variation of the output capacitance is often neglected, and an average value of the output capacitance is utilized in the energy-based method. As a result, although this method can achieve a better ZVS condition than the current-based method, parts of the calculated ZVS region could lead to hard switching in practice.

Regarding the charge-based method [65], the non-linearity of the output capacitance changing with the drain-source voltage is taken into account, resulting in a higher accuracy than the current- and energy-based methods. However, one drawback is the inappropriate calculation of the available charges in the leakage inductance current. In this method, the available charges are divided into two parts, and each part is calculated by integrating the bridge current from the zero-crossing point to the peak value. Then the obtained two charges are compared with the stored charge in the output capacitance to derive the ZVS condition. This calculation is not consistent with the practical switching transient, where the discharging of the turning-on power device might not start at the zero-crossing instant of the leakage inductance current (cf. Section 3.2). In other words, the integration time interval to calculate the available charges in the current is not appropriate. In addition, during the turning on transient, the assumption of half dc-bus voltage variation in [65] might not be proper, considering that the drain-source voltage of a power device is either zero or equal to the dc-bus voltage at the on-/off-state.

According to Chapter 2, the converter power transfer is determined by the phase-shift angle, and hence the ZVS limitation on the phase shift is of importance for the converter control. In the following, with varying phase shifts, the working waveforms during a practical switching transient are firstly introduced, followed by the analysis

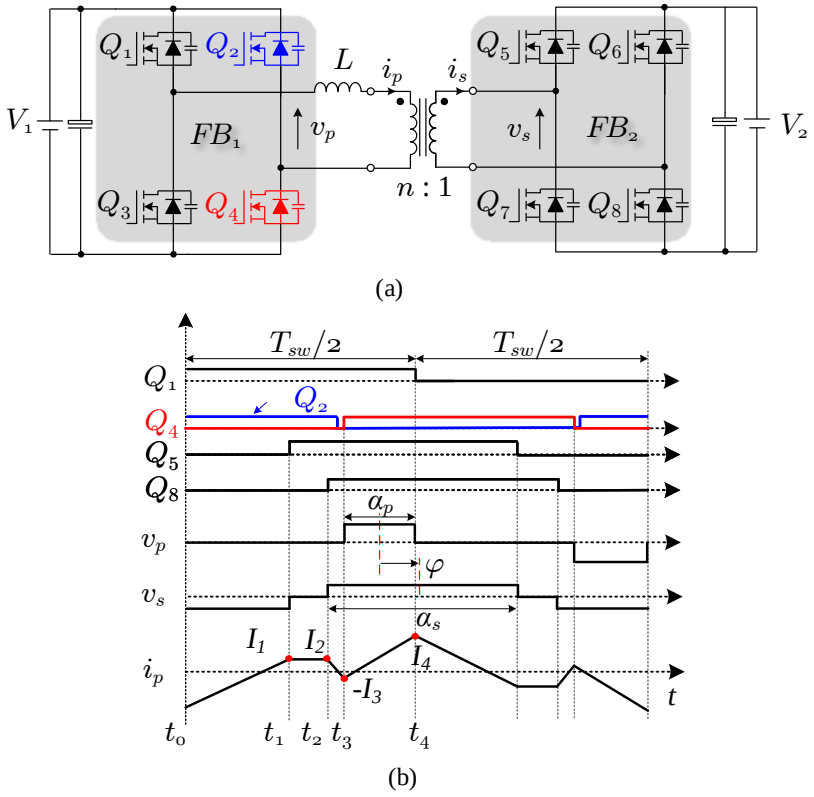


Fig. 3.2: Converter structure and operating (a) schematic diagram of the DAB topology and (b) waveforms of a typical light-load operation mode. [J2]

of the non-linear output capacitance and the dead time effect on the ZVS conditions. Then a comprehensive comparison among the proposed method and the prior-art methods is done with various system parameter configurations.

3.2 Practical Switching Transients

Corresponding to the DAB circuit in Fig. 3.2(a), the operating waveforms in light-load situation [66] are as shown in Fig. 3.2(b). There are three control variables in Fig. 3.2(b), namely the duty cycles of v_p, v_s and the phase shift between v_p and v_s, which are denoted by α_p, α_s and φ, respectively. Note that φ is defined as the phase shift between the fundamental components of the two high-frequency ac voltages. Due to that the switching signals for the two power devices in the same leg are complementary to each other, only four switching signals are depicted in Fig. 3.2(b).

In a power MOSFET, there are three parasitic capacitances interconnected among

Table 3.1: System Parameters of a DAB Prototype [J2]

Parameter	Variable	Value
Input DC voltage	V_1	200 V
Output DC voltage	V_2	35 V
Turns ratio of the transformer	$n:1$	3.5 : 1
Switching frequency	f_{sw}	60 kHz
Leakage inductance	L	45 μH
Dead time	T_{dead}	400 ns
Primary voltage duty ratio	α_p	160°
Secondary voltage duty ratio	α_s	80°

the gate, drain and source terminals due to the thin layer of silicon oxide [67], [68]. These parasitic capacitances are denoted by C_{GD}, C_{GS} and C_{DS} in the right inset of Fig. 3.3(a). In order to analyze the ZVS transient, the drain current is of high importance and thus the output capacitance $C_{oss} = C_{GD} + C_{DS}$ is often used to identify the drain-source voltage. Actually, C_{oss} is an equivalent capacitance by looking into the drain terminal of a MOSFET. Besides, it should be noted that the nonlinear trajectory of C_{oss} is almost fixed for a given power device and it does not change with the junction temperature. This is applicable to all power devices including the conventional Si super-junction [67] and the wide-band-gap GaN [69], [70] and SiC [71].

During the turning on of Q_4, namely around $t = t_3$ in Fig. 3.2(b), there are three switching transitions with different current flow paths and conducting components, as shown in Fig. 3.3(b) $\sim$ Fig. 3.3(d). In order to identify the practical ZVS boundary of Q_4, the measured switching transient waveforms including the drain-source voltage $V_{DS,Q4}$, the gate-source voltage $V_{GS,Q4}$ and the primary leakage inductance current i_p are shown in Fig. 3.4(a). The key experimental parameters of the utilized DAB setup are listed in Table 3.1. Note that some parameter values (e.g. the input dc voltage) might be selected differently from Table 2.1 in order to achieve a clear comparison among various experimental results. In Fig. 3.4(a), 8 experimental cases with varied phase-shift φ from 3° to 10° are presented, and for a clear view, 3 cases of them (i.e. $\varphi = 6°, 9°, 10°$) are extracted and shown in Fig. 3.4(b) $\sim$ Fig. 3.4(d), respectively.

The used power device of Q_4 is Infineon IPW65R080CFD, the threshold voltage of which is $V_{GS(th)}$ = 4 V (according to the transfer characteristics described by I_D - V_{GS} curve in the data sheet). As shown in Fig. 3.4(a) $\sim$ Fig. 3.4(d), during the turning on of Q_4, the drain-source voltage $V_{DS,Q4}$ starts to decrease at $t = 0.2\ \mu s$ until it reaches 0 at $t = 0.6\ \mu s$. The decreasing drain-source voltage indicates that the output capacitance is being discharged. In the meantime, the gate-source voltage $V_{GS,Q4}$ is increasing and the power device is switched on when $V_{GS,Q4}$ is equal to $V_{GS(th)}$. Therefore, zero-voltage turn-on is achieved if the drain-source voltage has been reduced to 0 at this switching on instant (cf. Fig. 3.4(b) and Fig. 3.4(c)), otherwise hard switching occurs (cf. Fig. 3.4(d)).

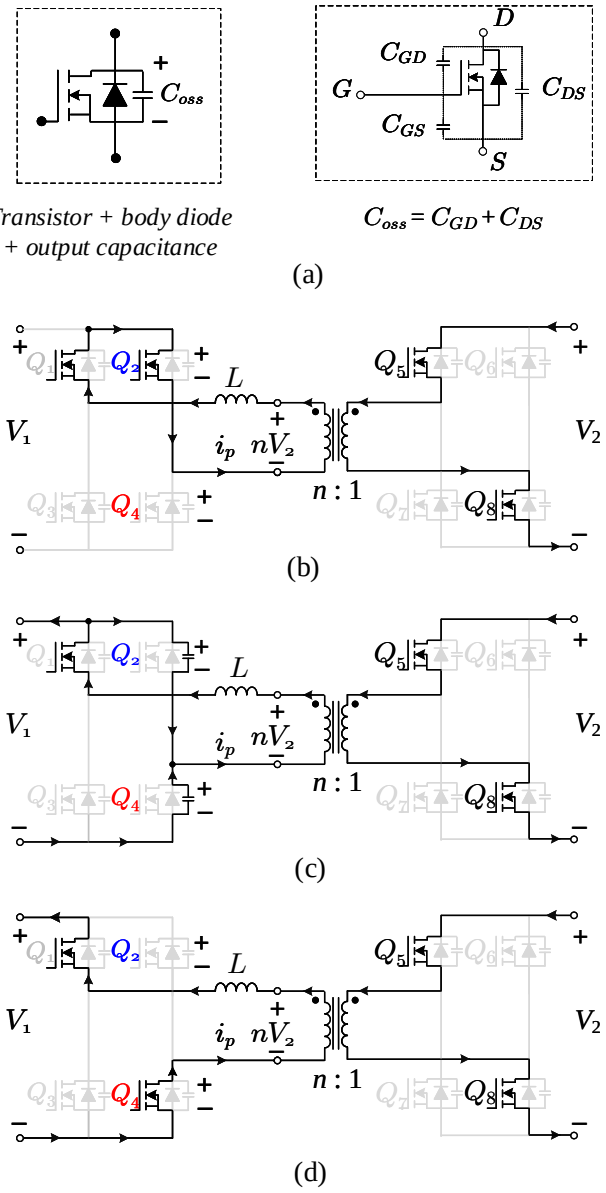


Fig. 3.3: Operation of the DAB converter (a) a general MOSFET parasitic model, and equivalent circuit states (b) before (c) during (d) after the turn-on of Q_4 transistor, which correspond to the time intervals $0 \sim 0.2\ \mu s$, $0.2\ \mu s \sim 0.6\ \mu s$ and $0.6\ \mu s \sim 1\ \mu s$ in Fig. 3.4(a), respectively.

According to the analysis above, it can be obtained that two conditions should be satisfied in order to realize soft turning on: *a)* the output capacitance should be totally

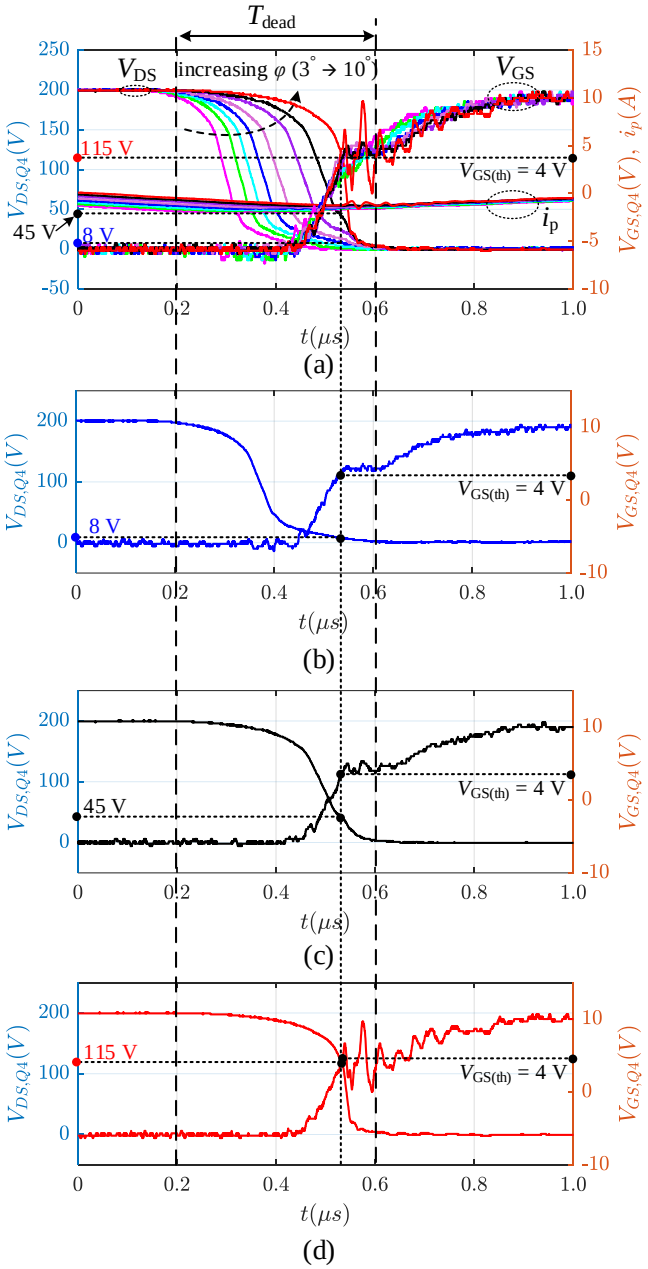


Fig. 3.4: Measured transient switching waveforms during the turning on of Q_4 (a) summarized experimental results of 8 cases with varying $\varphi = 3°, 4°...10°$ (b) extracted results with $\varphi = 6°$ (c) extracted results with $\varphi = 9°$ (b) extracted results with $\varphi = 10°$.

discharged before the turning on of Q_4 and *b)* the procedure of releasing charges to the leakage inductance current should be completed within the dead time.

3.3 Implementation of Nonlinear C_{oss} Profile

As analyzed in last section, the discharging/charging of the output capacitance (denoted by $C_{oss,Q4}$, $C_{oss,Q2}$) of Q_4 and Q_2 occur within the $V_{DS,Q4}$ varying period, namely the T_{dead} interval in Fig. 3.4. The equivalent circuit state associating with this interval is shown in Fig. 3.3(c). Therefore, the following transient expressions of $V_{DS,Q2}$ and $V_{DS,Q4}$ can be obtained.

$$\begin{cases} C_{oss,Q2}\dfrac{dV_{DS,Q2}}{dt} = -i_{D,Q2} \\ C_{oss,Q4}\dfrac{dV_{DS,Q4}}{dt} = i_{D,Q4} \end{cases} \tag{3.1}$$

Therein, $i_{D,Q2}$ and $i_{D,Q4}$ are the drain currents of Q_2 and Q_4, respectively. Applying Kirchhoff's Laws to the circuit in Fig. 3.3(c), there are

$$\begin{cases} i_{D,Q4} + i_{D,Q2} = i_p \\ V_{DS,Q4} + V_{DS,Q2} = V_1 \end{cases} \tag{3.2}$$

Combining (3.1) and (3.2) would have

$$i_p = \left[C_{oss,Q2} + C_{oss,Q4}\right]\frac{dV_{DS,Q4}}{dt} \tag{3.3}$$

Considering the non-linearity of the output capacitance C_{oss}, it could vary a lot depending on the drain-source voltage V_{DS}. Regarding the utilized Infineon IPW65R080CFD MOSFET power device in the DAB setup, the non-linear C_{oss} profile can be extracted from the datasheet or manually measured for each power device. In this thesis, the profile is directly from the datasheet, and due to the increasing $V_{DS,Q2}$ and decreasing $V_{DS,Q4}$ within the switching transition, the trajectories of $C_{oss,Q2}$ and $C_{oss,Q4}$ are shown in Fig. 3.5(a) and Fig. 3.5(b), respectively. For the convenience of analysis, an equivalent capacitance C_{eq} is introduced with

$$C_{eq} = C_{oss}(V_1 - V_{DS,Q4}) + C_{oss}(V_{DS,Q4}) \tag{3.4}$$

to replace the term $C_{oss,Q2} + C_{oss,Q4}$ in (3.3). Consequently, the C_{eq} profile can be obtained as in Fig. 3.5(c), and (3.3) can be transferred to

$$i_p = C_{eq}\frac{dV_{DS,Q4}}{dt} \tag{3.5}$$

As the concluded ZVS conditions from the last section and considering (3.5), the soft turn-on of Q_4 is achieved only if

$$Q_{ip} = \int_0^{T_{dead}} i_p dt \geq \int_0^{V_1} C_{eq} dV_{DS,Q4} = Q_{eq} \tag{3.6}$$

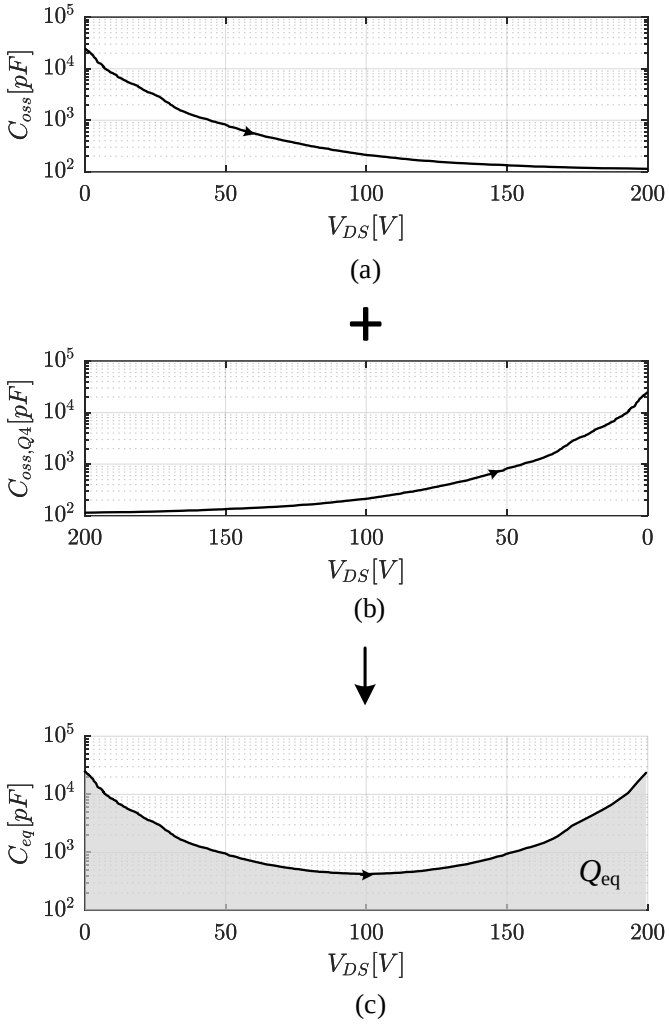


Fig. 3.5: Non-linear C_{oss} profiles for Infineon IPW65R080CFD (a) $C_{oss,Q2}$ trajectory (b) $C_{oss,Q4}$ trajectory (c) C_{eq} trajectory.

where Q_{ip} is the conveyed charges by the leakage inductance current i_p, and Q_{eq} is the stored charges in the equivalent capacitance C_{eq} with an off-state drain-source voltage V_1, which can be represented by the shaded area in Fig. 3.5(c).

With respect to the Q_{ip} in (3.6), it can be depicted by the patched area in Fig. 3.6(a), including the practical transient i_p waveforms in the same 8 cases in Fig. 3.4 and the waveforms of $V_{DS,Q4}$ in cases of $\varphi = 6°, 10°$. For a clear view, the Q_{ip} areas in the cases of $\varphi = 6°$ and $\varphi = 10°$ are extracted and shown in Fig. 3.6(b) and Fig. 3.6(c), respectively. Seen from Fig. 3.6(a) $\sim$ Fig. 3.6(c), the value of Q_{ip} decreases as φ is increased from 3° to 10°. If the instant $t = 0.6\ \mu s$ is deemed the start point

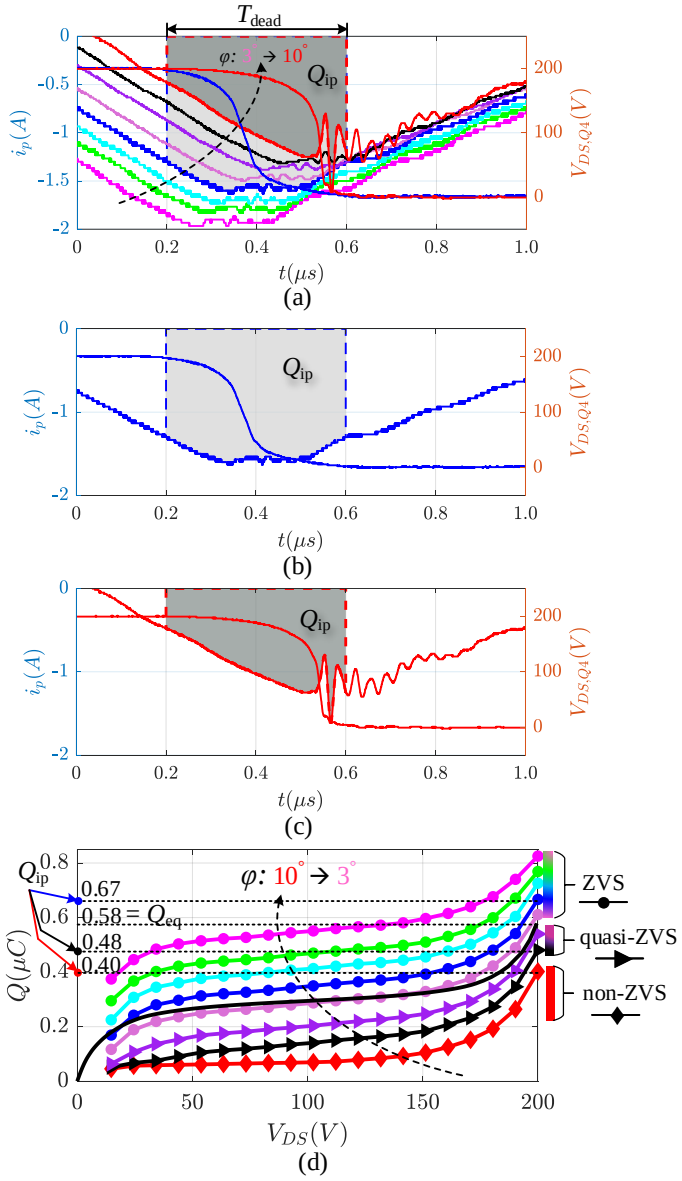


Fig. 3.6: Measured switching transient waveforms of (a) the leakage inductance currents i_p with $\varphi = 3^\circ \sim 10^\circ$ and the drain-source voltages $V_{DS,Q4}$ with $\varphi = 6^\circ, 10^\circ$ at the turning on of Q_4 (b) the extracted results with $\varphi = 6^\circ$ (c) the extracted results with $\varphi = 10^\circ$, and (d) the numerical integration (i.e. marked lines) of the measured i_p and the transient charge stored in C_{eq} (i.e. solid line). [J2]

of the dead time T_{dead} and $t = 0.2\ \mu s$ the end point, the drain-source voltage $V_{DS,Q4}$ would change reversely from 0 to V_1, and simultaneously, the conveyed charges Q by i_p during the switching transient can be calculated with the i_p experimental data. Thus the trajectories of Q with different φ can be achieved and they are shown in Fig. 3.6(d). As comparison, the transient charges stored in C_{eq} (cf. Fig. 3.5(c)) are also shown in Fig. 3.6(d), denoted by the solid curve with a final value of $Q_{eq} = 0.58\ \mu C$.

In cases of $\varphi = 3°...7°$, the charge Q_{ip} conveyed by the leakage inductance current i_p can be obtained using numerical integration technique. For example, as shown in Fig. 3.6(b), Q_{ip} is equal to 0.67 μC in the case of $\varphi = 6°$, and it is larger than the charge $Q_{eq} = 0.58\ \mu C$ in the equivalent capacitance. Therefore, the stored charges in C_{eq} can be fully released into the leakage inductance current and ZVS is achieved.

As φ increases, the conveyed charge by the current is decreased seen from the shaded areas in Fig. 3.6(a). When φ is equal to 10°, Q_{ip} can be similarly calculated from Fig. 3.6(c), which is 0.4 μC and lower than the stored charge $Q_{eq} = 0.58\ \mu C$. This indicates that C_{eq} can not be fully discharged before Q_4 is switched on and hard switching occurs. Consequently, seen from Fig. 3.4(d), the drain-source voltage $V_{DS,Q4}$ is dramatically dropped from 115 V to 0 V in less than 0.1 μs, and severe oscillations are induced in the the gate driving voltage $V_{GS,Q4}$ and the leakage inductance current i_p. This non-ZVS case should be avoided since it might increase the switching losses and even potentially break the power device [61] due to high dv/dt.

In terms of the middle cases where $\varphi = 8°, 9°$, the transferred charge Q_{ip} (equals 0.48 μC with $\varphi = 9°$) by the current is a bit lower than Q_{eq}, implying an insufficient discharge of C_{eq}. One difference from the 10° case is that the drain-source voltage of Q_4 has been reduced to a sufficient low level at turning on, e.g. 45 V for $\varphi = 9°$ (cf. Fig. 3.4(c)) and even lower for $\varphi = 8°$ (cf. Fig. 3.4(a)). Thus no obvious oscillations are stimulated and they are named as quasi-ZVS in Fig. 3.6(d). Even though quasi-ZVS would not impair the power device, it causes an increased switching losses and due to this, quasi-ZVS and non-ZVS are both regarded ZVS failure in the calculation of ZVS ranges in this chapter.

3.4 ZVS Range Calculation and Comparison

As shown in Fig. 3.1, there are mainly three approaches to derive the ZVS range in literature, namely the current-, energy- and charge-based methods, which are named as App1, App2 and App3 in the following. The proposed ZVS range calculation method is abbreviated by Pro.

App1: One popular way [62] to calculate the ZVS conditions in literature is by solving the leakage inductance current at the turn-on instant, and then it is compared with 0 to derive the ZVS limitations on the control variables. This approach does not take the output capacitance into account. As shown in Fig. 3.2(b), the shape of current i_p is determined by the voltage drop on the leakage inductance during the time interval $[t_i, t_{i+1}]$ (i = 0, 1, 2, 3) in a half switching period, which is

$$L \cdot \frac{di_p}{dt} = v_p - nv_s \tag{3.7}$$

Applying the volt-second balance principle to the leakage inductance, the absolute

values of i_p at $t = t_0$ and $t = t_4$ are identical. On this basis, the current at the turn-on instant of Q_4 can be calculated and the limitation on the control variables can be further obtained, as expressed by

$$I_3 = \frac{nV_2}{4\pi L f_{sw}}\left[(k-1)\alpha_p - 2\varphi\right] \geq 0 \rightarrow \alpha_p \geq \frac{2}{k-1}\varphi \tag{3.8}$$

where $k = V_1/(nV_2)$ is the input/output dc voltage ratio and f_{sw} is the switching frequency.

Noting that a more precise method of calculating i_p can be found in [41] if considering the effect of the resistive part (denoted by R_{eq}) in the passive components. In this case, (3.7) is rewritten as

$$L\frac{di_p(t)}{dt} + R_{eq}i_p(t) = v_p(t) - nv_s(t) \tag{3.9}$$

However, this would result in a more complex piecewise exponential i_p, rather than a piecewise linear i_p in (3.7). Although the calculation accuracy can be slightly improved, the complexity is considerably increased. Besides, the resistance of the circuit and the transformer is usually very small and can be neglected. Therefore, the calculation of I_3 is selected as in (3.8) in this chapter.

App2: Another conventional method [64], [72] to calculate the ZVS conditions is focusing on the energy exchange between the voltage sources and the leakage inductance during the turning on of Q_4. In this method, the output capacitance of Q_4 (cf. Fig. 3.5(b)) is regarded as a constant C_{con}, which is estimated as [64]

$$C_{con} = \frac{1}{V_1}\int_0^{V_1} C_{oss,Q4}dV_{DS} \tag{3.10}$$

Then the exchanged energy $E_{deliver}$ among the output capacitance and the dc voltage ports can be calculated using [72]

$$E_{deliver} = 2nC_{con}V_1V_2 - C_{con}V_1^2 \tag{3.11}$$

In order to achieve ZVS of Q_4, the minimum stored energy in i_p should be larger than $E_{deliver}$, and accordingly, the minimum value of I_3 (cf. Fig. 3.2(b)) can be further derived as

$$\frac{1}{2}LI_{3,min}^2 = E_{deliver} \xrightarrow{(3.11)} I_{3,min} = \sqrt{\frac{4nC_{con}V_1V_2 - 2C_{con}V_1^2}{L}} \tag{3.12}$$

Combined with the I_3 expression in (3.8), the ZVS limitation using the energy-based method can be achieved as

$$\alpha_p \geq \frac{2}{k-1}\varphi + \frac{4\pi L f_{sw}}{(k-1)nV_2}\sqrt{\frac{|\,4nC_{con}V_1V_2 - 2CV_1^2\,|}{L}} \tag{3.13}$$

App3: The third method [65] is comparing the stored charge in $C_{oss,Q4}$ (cf. Fig. 3.5(b)) with the two defined charges Q_A and Q_B in Fig. 3.7(a), namely

$$Q_{V_1} = \int_0^{V_1} C_{oss,Q4}dV_{DS} \geq max.\left\{Q_A = -\int_{t_{\theta x}}^{t_3} i_p dt, \quad Q_B = -\int_{t_3}^{t_{\theta y}} i_p dt\right\} \tag{3.14}$$

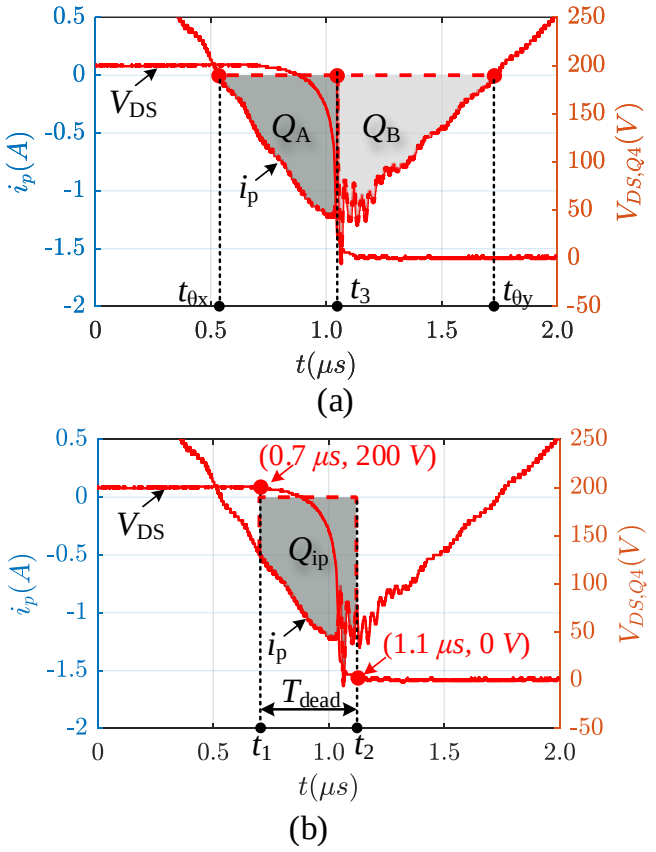


Fig. 3.7: Comparison of the i_p conveyed charges calculation between App.3 and the proposed method (a) the defined available charges Q_A and Q_B in App.3 (b) the defined Q_{ip} in Pro.. [J2]

Then the ZVS limitation can be further derived as

$$\alpha_p \geq max. \left\{ \begin{array}{c} \frac{2}{k-1}\varphi + \frac{4\pi f_{sw}}{k-1}\sqrt{\frac{LQ_{eq}}{nV_2}}, \\ \frac{2}{k-1}\varphi + \frac{4\pi f_{sw}}{k-1}\sqrt{\frac{(k-1)LQ_{eq}}{nV_2}} \end{array} \right\} \tag{3.15}$$

Although the non-linearity of the output capacitance is included in this method, the integration limits are not properly considered in (3.14). Seeing the two zero-crossing points in Fig. 3.7(a), the discharging of the output capacitance of Q_4 has not began at the first zero-crossing point ($t = t_{\theta x}$) and has finished at the second zero-crossing point (i.e. $t = t_{\theta y}$). Hence, the selected integration interval of this method to calculate the available charges in i_p is too wide. For example, using the experimental

data in Fig. 3.7(a), the values of Q_A and Q_B can be calculated with

$$\begin{cases} Q_A = 0.36\ \mu C > Q_{200V} = 0.29\ \mu C \\ Q_B = 0.44\ \mu C > Q_{200V} = 0.29\ \mu C \end{cases} \tag{3.16}$$

and it satisfies the ZVS requirement of (3.14), which means that this operating case (i.e. $\varphi = 10^\circ$) shown in Fig. 3.7(a) can achieve ZVS from the perspective of this method. However, the oscillation in Fig. 3.7(a) indicates that ZVS actually fails in this case.

As comparison, the considered Q_{ip} in the proposed method is shown in Fig. 3.7(b), where the integration limits are within $t_1 \sim t_2$, rather than the $t_{\theta x} \sim t_{\theta y}$ in Fig. 3.7(a). For ZVS verification purpose, there is

$$Q_{ip} = 0.4\ \mu C < Q_{eq} = 0.58\ \mu C \tag{3.17}$$

which does not satisfy the ZVS condition (3.6) and the i_p experimental result also agrees with this conclusion.

Pro.: Based on the previously practical ZVS analysis, the proposed method of deriving ZVS condition is to compare the stored charge in the equivalent capacitance C_{eq} with the conveyed charge in current i_p during transients, i.e. $Q_{ip} \geq Q_{eq}$ (cf. (3.6)). Seen from Fig. 3.6(d), the ZVS boundary is at $\varphi = 7^\circ$, and the relevant i_p and $V_{DS,Q4}$ working waveforms are extracted as shown in Fig. 3.8(a).

Based on the practical waveforms of i_p in Fig. 3.8(a), an approximate method to estimate Q_{ip} is by dividing the transient procedure into two intervals (cf. Fig. 3.8(b))

$$i_p = \begin{cases} -I_3,\ t \in \left[0, \dfrac{T_{dead}}{2}\right) \\ -I_3 + \dfrac{nV_2}{L}\left(t - \dfrac{T_{dead}}{2}\right), t \in \left[\dfrac{T_{dead}}{2}, T_{dead}\right] \end{cases} \tag{3.18}$$

and it results in

$$Q_{ip} = I_3 T_{dead} - \frac{nV_2 T_{dead}^2}{8L} \tag{3.19}$$

Hence, the ZVS limitation can be further derived with

$$\alpha_p \geq \frac{2}{k-1}\varphi + \frac{4\pi L f_{sw}}{(k-1)nV_2}\left[\frac{Q_{eq}}{T_{dead}} + \frac{nV_2}{8L}T_{dead}\right] \tag{3.20}$$

Based on the discussion above, the ZVS range of Q_4 can be depicted in an $\alpha_p - \varphi$ plane, as denoted by (3.8), (3.13), (3.15) and (3.20), which represent different calculation approaches. For a practical validation and comprehensive comparison, 24 experimental cases with different parameter configurations and various operating points are conducted and the results are depicted in Fig. 3.9. Details about the converter parameters from Config.1 $\sim$ Config.3 can be found in Table 3.2. The Config.1 has been analyzed previously, where φ is changed from 3° to 10° and the experimental ZVS boundary is at $\varphi_b = 7^\circ$ (cf. Fig. 3.6(d)). Here, φ_b is defined as the actual ZVS boundary obtained from the experiment, and the calculated boundary φ using different approaches are listed in the the last four columns of Table 3.2. Applying the same procedure as Config.1, the measured ZVS boundaries are found at $\varphi_b = 10^\circ$ and $\varphi_b = 12^\circ$ for Config.2 and Config.3, respectively. The varying range of φ is different

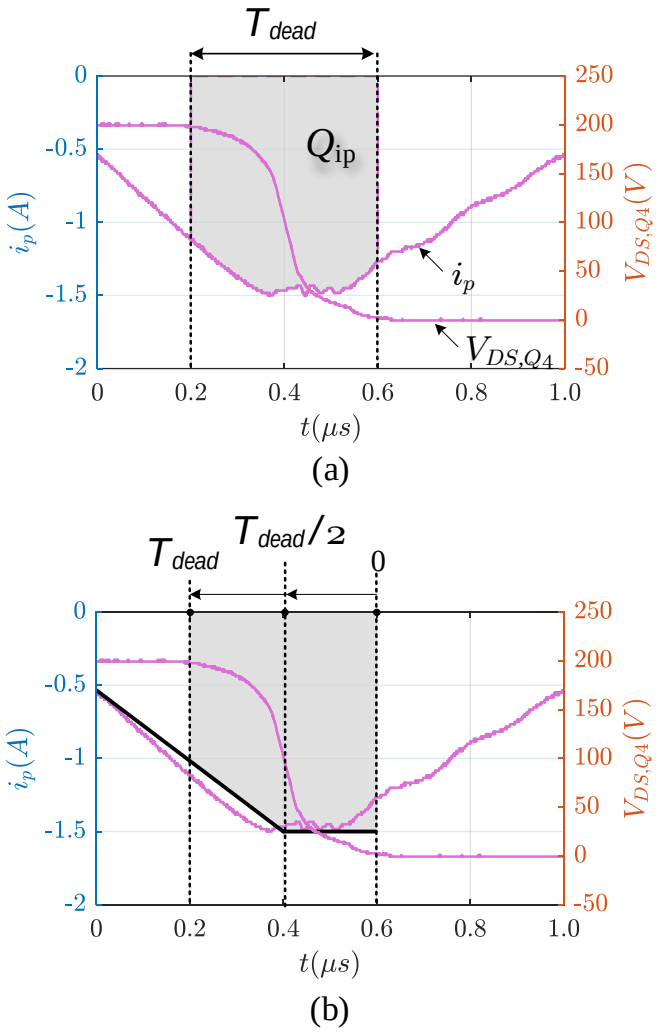


Fig. 3.8: Transient working waveforms in the ZVS boundary case of $\varphi = 7^\circ$ (a) the practical Q_{ip} (b) the estimation of Q_{ip} using linear approximation method.

from Config.1, where $6^\circ \sim 13^\circ$ and $9^\circ \sim 16^\circ$ are applied to Config.2 and Config.3, respectively. By comparing the actual φ_b with calculated boundary φ in Table 3.2, it can be seen that the proposed method has a higher accuracy.

In order to further verify the accuracy of proposed method, experiments with Config.4 $\sim$ Config.6 in Table 3.2 are implemented, where the input/output dc voltages differ from Config.1 $\sim$ Config.3. Corresponding to Config.4 $\sim$ Config.6, the transient working waveforms are illustrated in Fig. 3.10 $\sim$ Fig. 3.12, respectively. Similar to Fig. 3.6(d), the numerical integration result for each parameter configuration is depicted in

Table 3.2: Measured and Calculated ZVS Boundaries for Different System Parameter Configurations [J2]

Configs.	V_1	V_2	α_p	α_s	φ_b	App1	App2	App3	Pro.
Config.1	200 V	35 V	60°	110°	**7°**	19°	13°	11°	**6.4°**
Config.2	200 V	35 V	70°	140°	**10°**	22.2°	16.1°	14.2°	**9.6°**
Config.3	200 V	35 V	80°	160°	**12°**	25.3°	19.3°	17.4°	**12.8°**
Config.4	200 V	45 V	110°	160°	**5°**	14.8°	7.3°	6°	**5°**
Config.5	230 V	25 V	40°	150°	**16°**	32.6°	23.2°	17.6°	**15.4°**
Config.6	170 V	25 V	40°	150°	**5°**	18.9°	16.4°	8.6°	**5.6°**

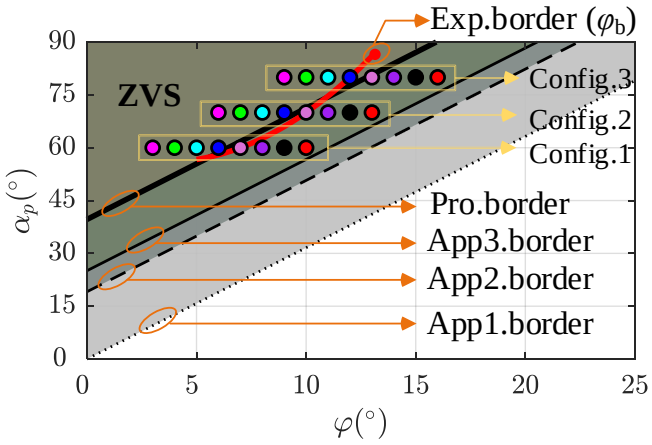


Fig. 3.9: Calculated ZVS boundaries of Q_4 using prior-art approaches $App1$, $App2$, $App3$ and the proposed method $Pro.$ with different system parameter configurations (cf. Table 3.2). Besides, experimental cases are denoted by marked points and the obtained experimental ZVS boundary is denoted by the red curve (i.e. Exp. border). [J2]

the bottom inset of Fig. 3.10 $\sim$ Fig. 3.12. Thus the experimental ZVS boundary can be obtained at $\varphi_b = 5°$, $\varphi_b = 16°$ and $\varphi_b = 5°$, respectively. Obviously, as summarized in Table 3.2, the calculated boundary φ with the proposed method is more close to φ_b than the other three calculation methods.

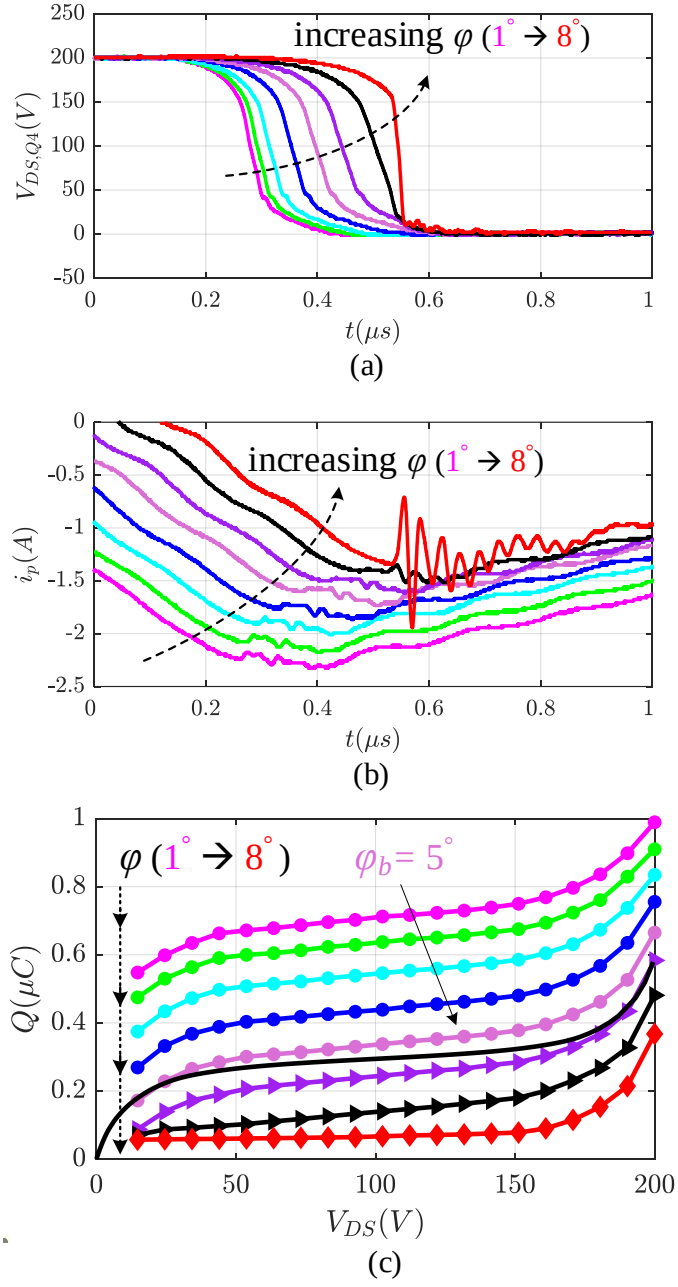


Fig. 3.10: In Config.4 (cf. Table 3.2), measured transients of (a) the drain-source voltage $V_{DS,Q4}$ and (b) the leakage inductance current i_p, and (c) the numerical integration of measured i_p.

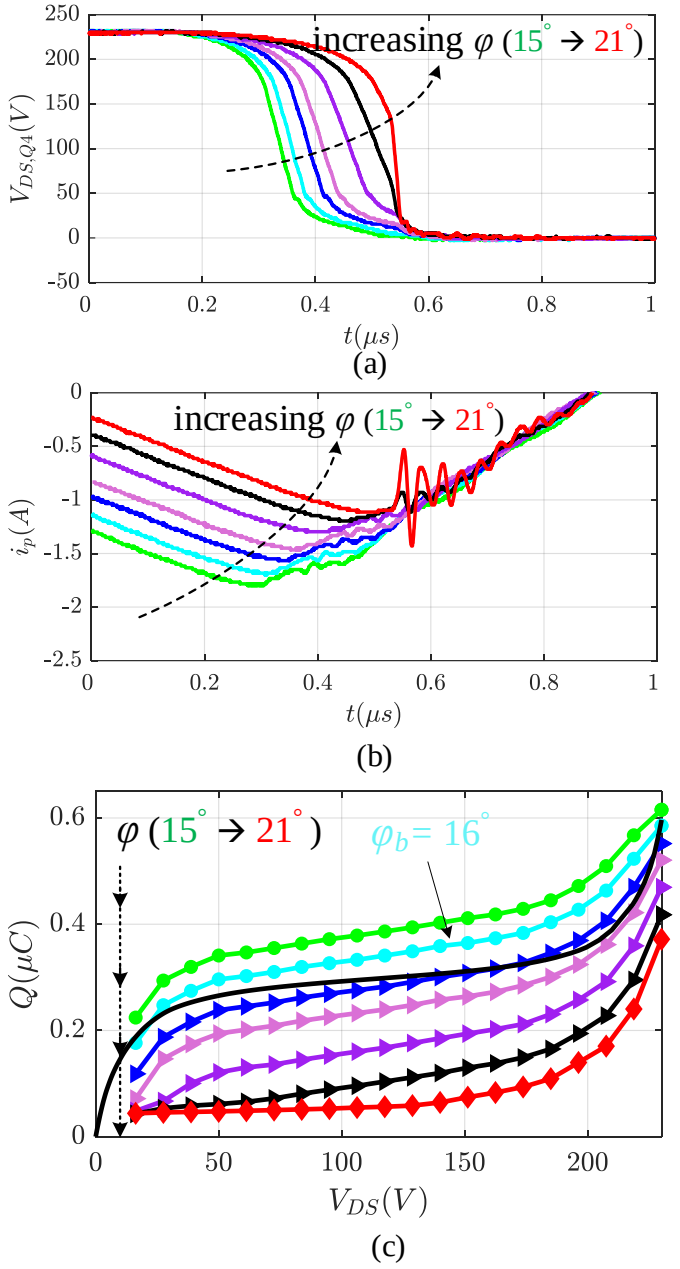


Fig. 3.11: In Config.5 (cf. Table 3.2), measured transients of (a) the drain-source voltage $V_{DS,Q4}$ and (b) the leakage inductance current i_p, and (c) the numerical integration of measured i_p.

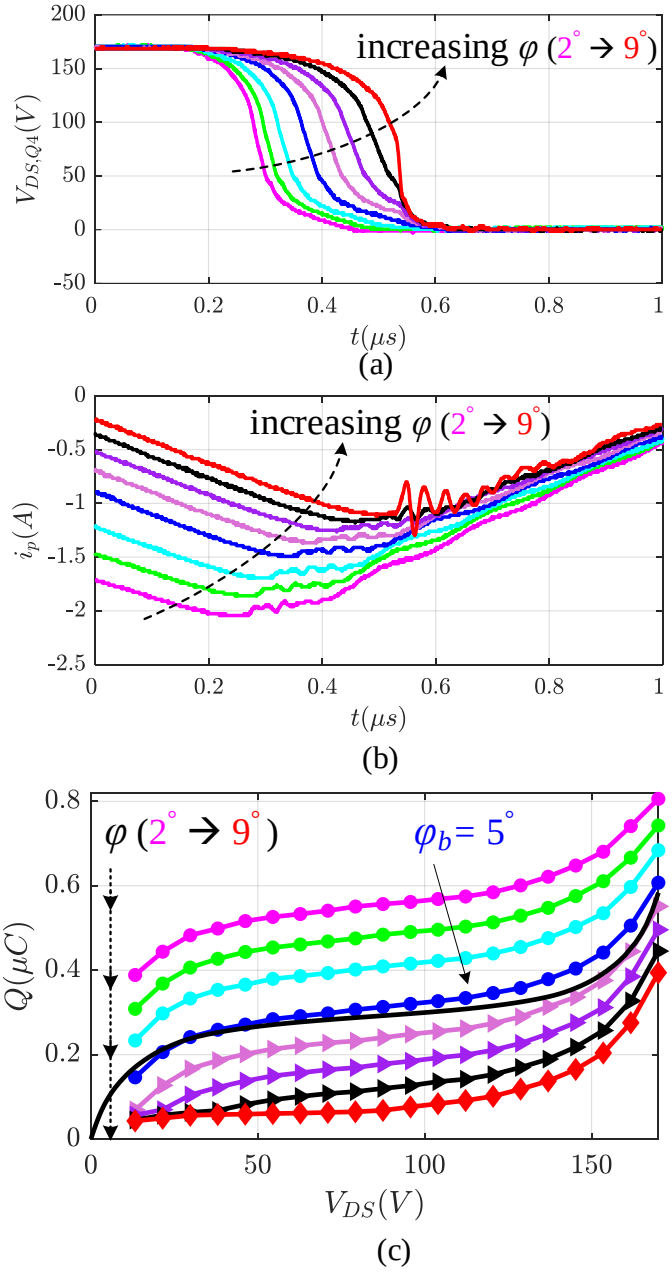


Fig. 3.12: In Config.6 (cf. Table 3.2), measured transients of (a) the drain-source voltage $V_{DS,Q4}$ and (b) the leakage inductance current i_p, and (c) the numerical integration of measured i_p.

3.5 Summary

Based on the practical measured switching transients and taking into account the non-linearity of output capacitance in the MOSFET, an accurate method of calculating the ZVS range is proposed in this chapter. Focusing on the dead time interval where the switching transition happens, the two power devices in the same leg are analyzed together by simultaneously considering the charging and discharging procedure. As a result, the concepts of equivalent output capacitance and equivalent charge are defined in order to conveniently analyze the ZVS transient and identify the ZVS boundary. As comparison, the prior-art methods of ZVS calculation are also introduced and it is proved that the proposed approach has a higher accuracy on forecasting the ZVS boundary. Experiments with different system parameter configurations are conducted and the results are consistent with the theoretical analysis.

Chapter 4

Advanced DAB Modulation Scheme

4.1 Background

Considering a practical OBC, the battery voltage usually varies in a wide range depending on the state-of-charge (SoC), and the charging power also varies a lot from light-load slow charging to the heavy-load fast charging, determined by the individual loading profile. However, in the earliest way to modulate the DAB converter [73], which is by regulating the phase-shift angle between the two bridge terminal voltages, the DAB is prone to lose ZVS in partial loading situations if the input/output dc voltage ratio deviates from 1 [74–79]. Hence, many improved modulation schemes are proposed to extend the DAB soft-switching operating range, which can be basically divided into four types as shown in Fig. 4.1.

The DAB converter circuit and relevant working waveforms with the triple-phase-shift (TPS) modulation scheme are shown in Fig. 4.2(a) and Fig. 4.2(b), respectively. Taking T_{sw} as the switching period in Fig. 4.2(b), the TPS has the highest three degrees of freedom, i.e. the two duty cycles D_p and D_s of respective primary (v_p) and secondary (v_s) bridge terminal voltages, and the phase-shift ratio D_φ between the fundamental components of these two voltages. Usually each power device in DAB is switched with a 50% duty ratio driving signals and the three control variables D_p, D_s and D_φ are regulated by controlling the phase-shift angles between these rectangular driving signals. For example, D_p is controlled by Q_1 and Q_4, and D_s by Q_5 and Q_8. Thus, D_p and D_s can be varied in the range of $[0,\ 1]$. Besides, D_φ is limited within $[0,\ 1/2]$ to reduce the conduction losses, which is explained in Section 4.3. On this basis, the four types of modulation schemes in Fig.4.1 can be divided by

a) Single-phase-shift (SPS) modulation [73]: $D_p = D_s = 1,\ 0 < D_\varphi < 1/2$.

b) Extended-phase-shift (EPS) modulation [80]: $D_p = 1,\ 0 < D_s < 1,\ 0 < D_\varphi < 1/2$ or $D_s = 1,\ 0 < D_p < 1,\ 0 < D_\varphi < 1/2$.

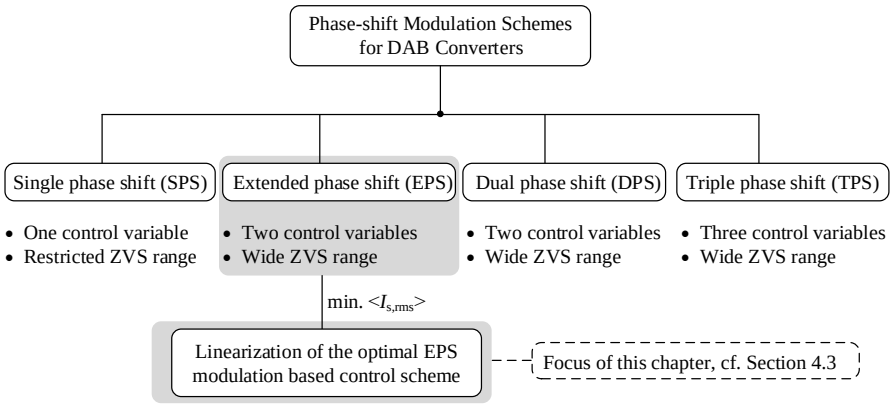


Fig. 4.1: Prior-art modulation schemes (i.e. SPS, EPS, DPS, TPS) and the proposed optimized modulation scheme in this chapter.

c) Double-phase-shift (DPS) modulation [81, 82]: $0 < D_p = D_s < 1$, $0 < D_\varphi < 1/2$.

d) Triple-phase-shift (TPS) modulation [83–86]: $0 < D_p < 1$, $0 < D_s < 1$, $0 < D_\varphi < 1/2$.

It can be seen that instead of using only one control variable in the earliest SPS modulation, the other improved modulation schemes use more to optimize the converter performance from multiple perspectives, such as the extension of the ZVS range and the reduction of current stress [87–91], reverse power flow [92] and non-active power loss [93]. Essentially, these optimization targets are realized by regulating the leakage inductance current, e.g. current stress reduction is usually achieved by reducing the current peak value, and backflow power minimization often refers to shortening the time interval during which the current flows back to the power source. On this basis, much research are focused on reducing the root mean square (RMS) value of the leakage inductance current [94–97] for the sake of conduction loss optimization. In addition to the control variables above, another degree of freedom - the switching frequency - can also be regulated [21, 98] to achieve particular optimization objectives.

However, more control variables might complicate the control and thus even become difficult to implement in practical situations. In order to operate the DAB converter at the optimal point, massive on-line calculations are needed to solve the optimal control variables, and meanwhile the other converter performances such as the ZVS range and maximum power transfer should not be sacrificed. One usual way to reduce the computational burden is utilizing a look-up table to store the optimal control points, which are often calculated off-line based on different output power levels. But the control accuracy is easy to lose due to component aging, temperature-dependent component parameters (e.g. on-state resistance) deviation and also external disturbance.

This chapter will introduce an optimized hybrid modulation scheme targeting at

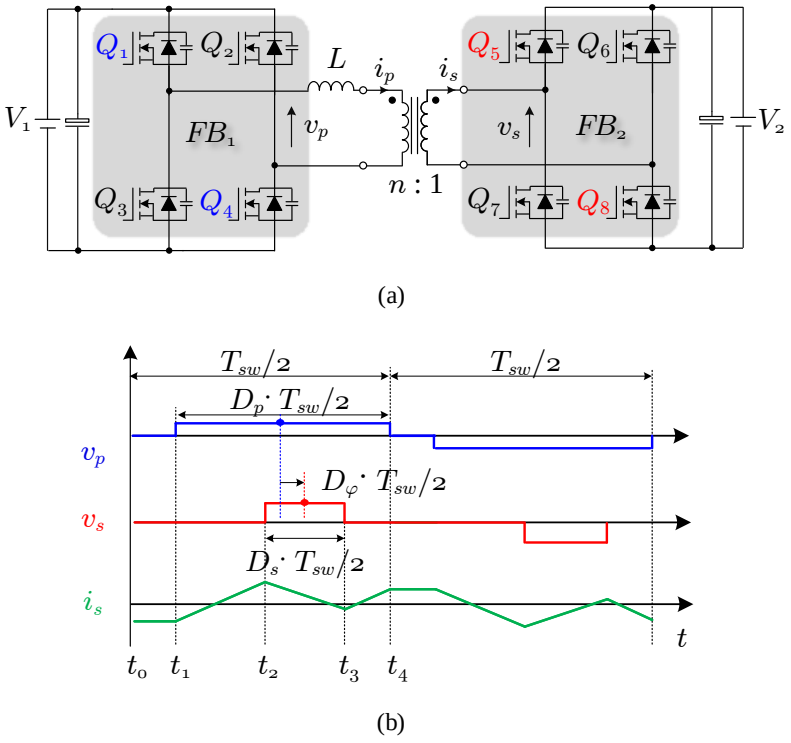


Fig. 4.2: DAB and its operation (a) Circuit of the DAB topology (b) Working waveforms of the DAB converter with triple-phase-shift (TPS) modulation scheme. [J1]

reducing the conduction losses and meanwhile simplifying the on-line control, which is achieved by linearizing the optimal EPS modulation based control scheme. In the following, the losses distribution on different components are calculated at first and then the EPS modulation scheme is introduced, followed by the linearization of the optimal EPS based control strategy with experimental validation.

4.2 Losses Distribution in DAB

The power losses in a DAB converter can basically be classified into *A)* the copper losses and core losses of the magnetic components, *B)* the conduction losses and switching losses of the power devices, *C)* the resistive losses in the dc-link capacitors. In the following, the calculation principle of these loss sources are introduced separately, and then the percentages of each loss source over the total losses are calculated for the built DAB setup, which is operated in various loading situations.

A. High-Frequency Transformer and the Cascaded Auxiliary Inductor

Table 4.1: Components and Relevant Parameters of the Built DAB Prototype [J1]

Components	Parameters
Primary winding of the HF transformer: 35 turns copper foil	R_{Trp}=607.9 mΩ @T_a=25 °C
Secondary winding of the HF transformer: 10 turns copper foil	R_{Trs}=16.5 mΩ @T_a=25 °C
Auxiliary inductor: 10 turns Litz wire, 20 strands, strand diameter = 0.355 mm	R_L=27.9 mΩ @T_a=25 °C
MOSFETs $Q_1 \sim Q_4$: IPW65R080CFD	R_{DSonp}=72 mΩ @T_j=25 °C
MOSFETs $Q_5 \sim Q_8$: 2 x IPP110N20N3 in parallel	R_{DSons}=9.6 mΩ @T_j=25 °C

In the built DAB setup, an inductor is in series with the primary winding of the high-frequency (HF) isolated transformer, which can be regarded as a part of the total leakage inductance. The losses caused by these magnetic components (i.e. the auxiliary inductor and the transformer) mainly comprise copper losses and core losses. Given the parameters in Table 4.1, the copper losses (i.e. resistive losses) can be calculated with

$$P_{cond,Tr} = \left(\frac{R_L + R_{Trp}}{n^2} + R_{Trs}\right) \cdot I_{s,rms}^2 \tag{4.1}$$

where R_L is the resistance of the auxiliary inductor, R_{Trp} and R_{Trs} of the respective primary and secondary winding of the transformer, n is the turns ratio from primary to secondary side of the transformer, and $I_{s,rms}$ is the RMS leakage inductance current referring to the secondary side.

With respect to the core losses calculation, Steinmetz equation [99] can be employed if assuming a fundamental sinusoidal current instead of the actual piecewise linear current. The core loss per unit volume is

$$p_v = C_m f_{sw}^{\alpha} \hat{B}^{\beta} \tag{4.2}$$

and the core volumes of the transformer and inductor are V_{Tr} and V_L, respectively. In (4.2), the peak magnetic flux density $\hat{B}$ of the transformer can be estimated with $\hat{B}_{Tr} \approx 2V_1/(\pi^2 f_{sw} N_{Trp} A_{Tr})$ (N_{trp}: primary winding turns, A_{Tr}: effective magnetic cross section) and the inductor with $\hat{B}_L \approx \mu_{eff}\mu_0 N_L \hat{I}_L / l_L$ (μ_{eff}: equivalent relative permeability of the gapped core, N_L: winding turns, $\hat{I}_L$: peak inductor current, l_L: effective magnetic path length). The values of these magnetic parameters can be found in Table 4.2.

B. Power Devices

Table 4.2: Magnetic Core Parameters [J1]

Transformer (core type: ETD59/31/22, material: N97)					
V_{Tr}	A_{Tr}	N_{Trp}	C_m	α	β
51.2 cm^2	368 mm^2	35	8.21	1.28	2.2
Auxiliary Inductor (core type: ETD44/22/15, material: N87)					
V_L	l_L	μ_{eff}	C_m	α	β
17.8 cm^2	10.3 cm	120	10	1.26	2.15

The power losses of power devices include conduction losses and switching losses. Therein, the conduction losses can be calculated by

$$P_{cond,sw} = 4 \cdot \frac{R_{DSonp}}{N_{swp}} \cdot \left(\frac{I_{s,rms}}{\sqrt{2}n}\right)^2 + 4 \cdot \frac{R_{DSons}}{N_{sws}} \cdot \left(\frac{I_{s,rms}}{\sqrt{2}}\right)^2 \tag{4.3}$$

with $I_{s,rms}$ as the RMS value of the leakage inductance current. R_{DSonp} and R_{DSons} are the on-state resistance of the primary and secondary power device, respectively. N_{swp} and N_{sws} are the number of the paralleled power devices for each switch in the primary and secondary full bridge, respectively.

In terms of the switching losses calculation, the turn-on losses are neglected due to the ZVS achievement, and only turn-off losses are considered for each transistor, which can be estimated by [100]

$$p_{sw} = U_{DS} \cdot I_{off} \cdot \frac{t_{ru} + t_{fi}}{2} \cdot f_{sw} \tag{4.4}$$

where U_{DS} denotes the off-state drain-source voltage and I_{off} is the drain current at turning off. t_{ru} and t_{fi} are the rise time and fall time during turn-off transients.

C. *Capacitors*

The losses dissipated in the capacitors can be calculated with

$$p_{cap} = \frac{R_{ESR}}{N_{cap}} I_c^2 \tag{4.5}$$

where R_{ESR} is the the equivalent series resistance (ESR), N_{cap} is the number of paralleled capacitors and I_c is the RMS capacitor current during one switching period. In the built setup, one TDK B43544A6397M000 (C_1=0.39 mF) is used on the dc input side and five TDK EETEE2D301HJ in parallel (C_2=1.5 mF) on the dc output.

Based on the discussions above, the total power losses P_{total} can be categorized into switching losses P_{sw}, conduction losses P_{cond}, core losses P_{core} and capacitor losses P_{cap}, namely

$$P_{total} = P_{sw} + P_{cond} + P_{core} + P_{cap} \tag{4.6}$$

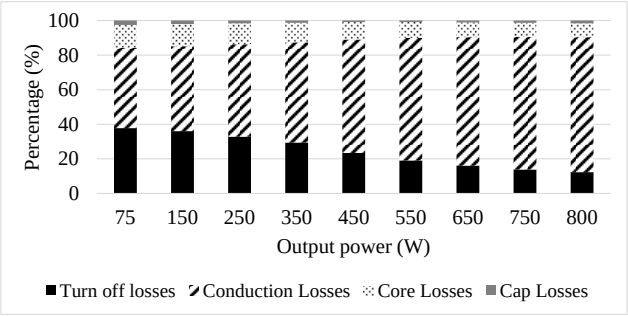


Fig. 4.3: Power loss distribution for different loss types. [J1]

with further specifications:

$$\begin{aligned} P_{sw} &= P_{sw,Q_1\sim Q_4} + P_{sw,Q_5\sim Q_8} \\ P_{cond} &= P_{cond,Tr} + P_{cond,sw} \\ P_{core} &= P_{core,Tr} + P_{core,L} \\ P_{cap} &= P_{cap,in} + P_{cap,out} \end{aligned} \tag{4.7}$$

By operating the converter under different loading situations, the calculated loss percentages are shown in Fig. 4.3. It can be seen that the conduction losses dominate the total power losses due to the ZVS achievement. Therefore, reducing the conduction losses is of high importance to benefit the power conversion efficiency.

4.3 Optimal EPS Modulation Scheme

Seen from the conduction losses calculation (4.1) and (4.3), the conduction losses are dependent on the RMS leakage inductance current. Hence, in the following, the operating modes of extended phase-shift (EPS) modulation and the calculation of the RMS current are firstly introduced. Then the analytical optimal operating points to achieve minimum conduction losses at various output power levels are analyzed.

4.3.1 Operating Modes with EPS

For the convenience of analysis, the DAB converter in Fig. 4.2(a) can usually be modeled by Fig. 4.4. Besides, the voltage ratio k, the base power P_b and the base current I_b are introduced with

$$k = \frac{V_1}{nV_2}, \quad P_b = \frac{(nV_2)^2}{8Lf_{sw}}, \quad I_b = \frac{n^2V_2}{8Lf_{sw}} \tag{4.8}$$

In order to define the varying range of the phase shift angle between the two full-bridges in a DAB converter, the original SPS working waveforms in Fig. 4.5(a) ($\varphi =$

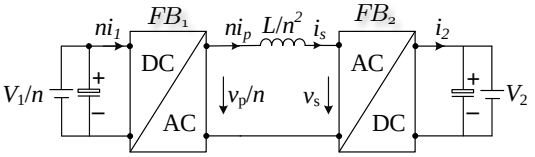


Fig. 4.4: Simplified DAB model by referring to the secondary side of the the transformer. [J1]

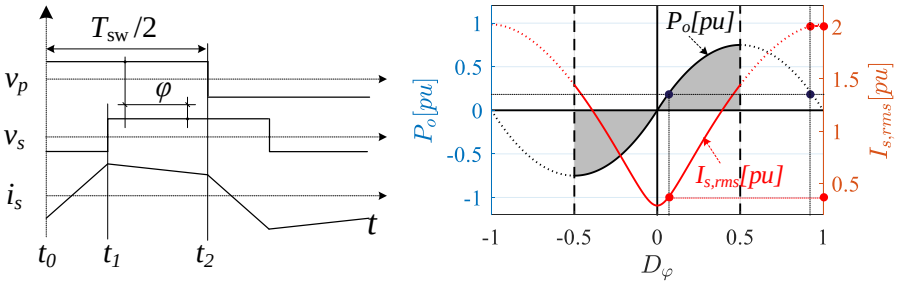


Fig. 4.5: In single-phase-shift modulation, (a) working waveforms (b) the normalized output power $P_o[pu]$ and RMS leakage inductance current $I_{s,rms}[pu]$ varying with the phase-shift D_φ. [J1]

πD_φ) are firstly utilized to calculate the normalized output power P_o and RMS current $I_{s,rms}$, which are

$$\begin{cases} P_o[pu] = 1/P_b \cdot 1/T_{sw} \cdot \int_0^{T_{sw}} [v_s(t) \cdot i_s(t)]dt = 4kD_\varphi(1-D_\varphi) \\ I_{s,rms}[pu] = 1/I_b \cdot \sqrt{1/T_{sw} \cdot \int_0^{T_{sw}} i_s^2(t)dt} = \dfrac{2\sqrt{3}}{3} \cdot \sqrt{(12D_\varphi^2 - 8D_\varphi^3 - 2)k + k^2 + 1} \end{cases} \tag{4.9}$$

Based on (4.9), the P_o and $I_{s,rms}$ trajectories ($k = 0.75$) along with D_φ can be characterized as in Fig. 4.5(b). Positive D_φ means a forward power flow from primary to secondary and negative means the reverse direction. In the positive range of $[0,\ 1]$, the power trajectory is symmetrical in the ranges of $D_\varphi \in [0,\ 0.5]$ and $D_\varphi \in [0.5,\ 1]$, but a lower $I_{s,rms}$ is achieved with $D_\varphi \in [0,\ 0.5]$. Therefore, D_φ is limited within $[0,\ 0.5]$ in most phase-shift modulation schemes.

As discussed in Section 4.1, if the duty cycle D_α of either v_p or v_s is varied (instead of constant in SPS), the modulation scheme transfers to EPS, and four operating modes can be obtained, as shown in Fig. 4.6 ($\alpha = \pi D_\alpha$). Therein, Mode I and Mode II are applicable for voltage boost scenarios (i.e. $k < 1$), and Mode III and Mode IV for voltage buck scenarios (i.e. $k > 1$). Similarly, the normalized output power and RMS leakage inductance current can be calculated as summarized in Table 4.3.

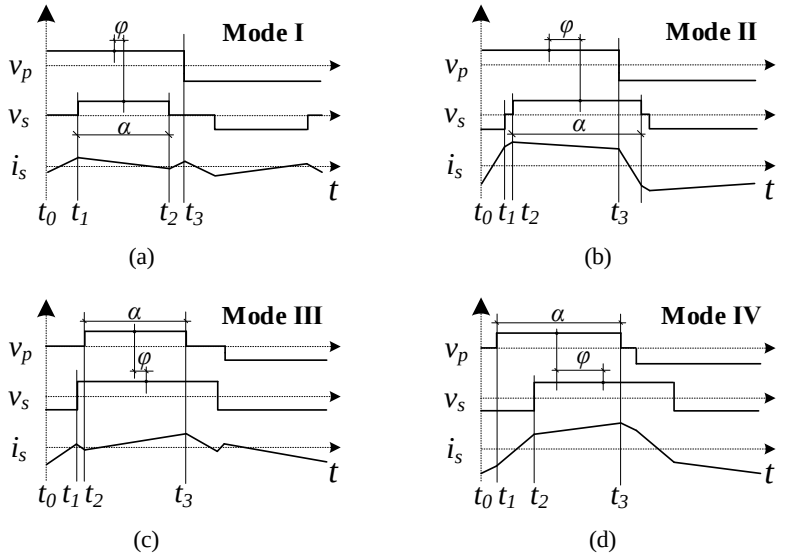


Fig. 4.6: EPS working wavefroms depending on the voltage ratio k and the two control variables D_α and D_φ (a) Mode I: $k < 1$, $D_\varphi < (1 - D_\alpha)/2$, (b) Mode II: $k < 1$, $D_\varphi > (1 - D_\alpha)/2$, (c) Mode III: $k > 1$, $D_\varphi < (1 - D_\alpha)/2$, (d) Mode IV: $k > 1$, $D_\varphi > (1 - D_\alpha)/2$. [J1]

4.3.2 ZVS Range

In the ZVS of a power device, the body diode is conducting before the transistor is turned on, which means that the current direction is from the source to drain of a MOSFET at the turning on instant. On this basis, the ZVS conditions for each operation mode in Fig. 4.6 can be derived, which are

$$\begin{cases} \dfrac{2k}{1-k} D_\varphi < D_\alpha < k, \quad 0 < D_\varphi < \dfrac{1-k}{2} & \longleftarrow \text{Mode I} \\ D_\alpha > \dfrac{2k(1-D_\varphi)}{1+k}, \quad \dfrac{1-k}{2} < D_\varphi < \dfrac{1}{2} & \longleftarrow \text{Mode II} \\ \dfrac{2}{k-1} D_\varphi < D_\alpha < \dfrac{1}{k}, \quad 0 < D_\varphi < \dfrac{k-1}{2k} & \longleftarrow \text{Mode III} \\ D_\alpha > \dfrac{2(1-D_\varphi)}{1+k}, \quad \dfrac{k-1}{2k} < D_\varphi < \dfrac{1}{2} & \longleftarrow \text{Mode IV} \end{cases} \tag{4.10}$$

4.3.3 Conduction Losses Minimization

Seen from the power expression in Table 4.3, different D_α and D_φ might lead to the same output power, and this facilitates the minimization of the conduction losses by operating the converter at the optimal combination of D_α and D_φ. For example, Fig. 4.7(a) and Fig. 4.7(b) illustrate the operating waveforms with the same output power

Table 4.3: Expressions of the Normalized RMS Leakage Inductance Current and Output Power [J1]

Mode	$I_{s,rms}[pu]$	$P_o[pu]$
Mode I	$\frac{2}{3}\cdot sqrt\Big[3(k-2)D_\alpha^3+9D_\alpha^2$ $+(36D_\varphi^2-9)kD_\alpha+3k^2\Big]$	$4kD_\alpha D_\varphi$
Mode II	$\frac{2}{3}\cdot sqrt\Big[-6D_\alpha^3+(-18kD_\varphi+9k+9)D_\alpha^2$ $+(36D_\varphi-18)kD_\alpha+3k^2+3k(1-2D_\varphi)^3\Big]$	$-k[4D_\varphi^2-4D_\varphi$ $+(1-D_\alpha)^2]$
Mode III	$\frac{2}{3}\cdot sqrt\Big[3-(6k^2-3k)D_\alpha^3+9k^2D_\alpha^2$ $-3kD_\alpha(3-12D_\varphi^2)\Big]$	$4kD_\alpha D_\varphi$
Mode IV	$\frac{2}{3}\cdot sqrt\Big[-6k^2D_\alpha^3+(9k^2-18kD_\varphi+9k)D_\alpha^2$ $-(18-36D_\varphi)kD_\alpha+3-3(1-2D_\varphi)^3k\Big]$	$-k[4D_\varphi^2-4D_\varphi$ $+(1-D_\alpha)^2]$

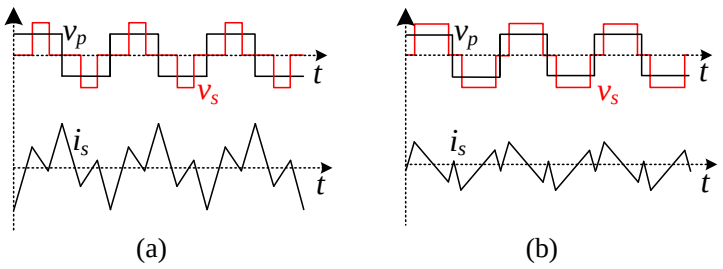


Fig. 4.7: Simulated working waveforms for the same output power with different combinations of (a) $D_\alpha = 0.35$, $D_\varphi = 0.053$ (b) $D_\alpha = 0.73$, $D_\varphi = 0.026$. [J1]

but with different combinations of D_α and D_φ. Obviously, the RMS value of the leakage inductance current in Fig. 4.7(b) is smaller.

Combining the expressions of $I_{s,rms}$ and P_o in Table 4.3, the optimal relationship function between D_α and D_φ (i.e. $D_{\alpha,opt} = f(D_\varphi)$) to achieve the minimum RMS

current can be derived as

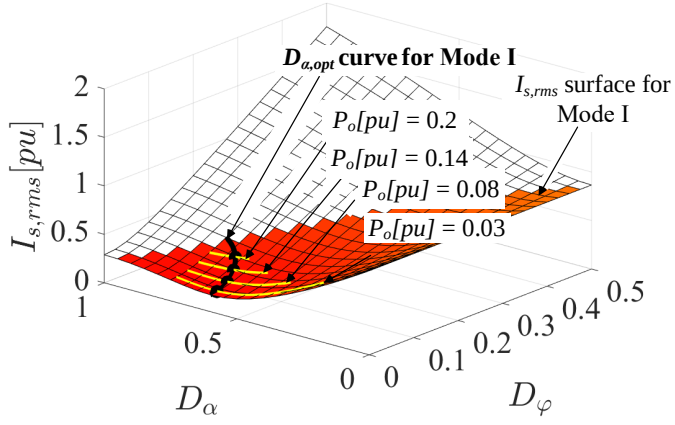
$$\begin{cases} D_{\alpha,opt} = \frac{1-\sqrt{(1-k)^2-4k(2-k)D_\varphi^2}}{2-k}, & D_\varphi \in \left[0, \quad \frac{1-k}{2}\right] \quad \longleftarrow \text{Mode I (EPS)} \\ D_{\alpha,opt} = \frac{2D_\varphi+k-1+\sqrt{(1-k-2D_\varphi)^2+[k(1-2D_\varphi)]^2}}{k}, & \\ \qquad\qquad for \quad D_\varphi \in \left[\frac{1-k}{2}, \quad \frac{k-1+\sqrt{1-k^2}}{2k}\right] \quad \longleftarrow \text{Mode II (EPS)} & \\ D_{\alpha,opt} = 1, \qquad for \quad D_\varphi \in \left[\frac{k-1+\sqrt{1-k^2}}{2k}, \quad \frac{1}{2}\right] \quad \longleftarrow \text{Mode II (SPS)} & \\ D_{\alpha,opt} = \frac{k-\sqrt{(k-1)^2-4(2k-1)D_\varphi^2}}{2k-1}, & D_\varphi \in \left[0, \quad \frac{k-1}{2k}\right] \quad \longleftarrow \text{Mode III (EPS)} \\ D_{\alpha,opt} = kD_\varphi - k + 1 + \sqrt{[(1-2D_\varphi)k-1]^2+(1-2D_\varphi)^2}, & \\ \qquad\qquad for \quad D_\varphi \in \left[\frac{k-1}{2k}, \quad \frac{1-k+\sqrt{k^2-1}}{2}\right] \quad \longleftarrow \text{Mode IV (EPS)} & \\ D_{\alpha,opt} = 1, \qquad for \quad D_\varphi \in \left[\frac{1-k+\sqrt{k^2-1}}{2}, \quad \frac{1}{2}\right] \quad \longleftarrow \text{Mode IV (SPS)} & \end{cases} \tag{4.11}$$

It can be seen that in Mode II and Mode IV, the optimal relationship function $D_{\alpha,opt} = f(D_\varphi)$ is different depending on the D_φ range. Especially, if D_φ is close to 0.5, the optimal D_α is located at 1, indicating that the EPS transfers to SPS. In order for a visual distinction, the $I_{s,rms}$ surfaces varying with D_α and D_φ are depicted in Fig. 4.8. Besides, the $D_{\alpha,opt}$ curves varying with D_φ (cf. (4.11)) and the power curves $P_o = f(D_\alpha, D_\varphi)$ (cf. Table 4.3) are also plotted on the $I_{s,rms}$ surfaces. Consequently, the intersection points of the $D_{\alpha,opt}$ curves and the P_o curves are the optimal operating points, as shown by the black points in Fig. 4.8. For each power curve, the intersection point results in the minimum $I_{s,rms}$, which validates the correctness of (4.11).

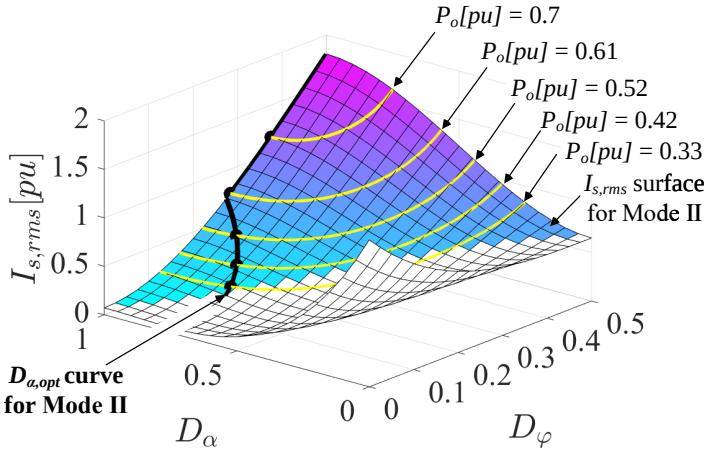
Taking the ZVS range into account, the $I_{s,rms}$ surfaces in Fig. 4.8 can be mapped into the $D_\alpha - D_\varphi$ plane in Fig. 4.9(a), corresponding to Mode I and Mode II in the boost scenarios. Regarding the other two operating modes (Mode III, Mode IV) in the buck scenario, a similar Fig. 4.9(b) is can be obtained. It can be seen that the optimal operating points ares located within the ZVS regions, which implies that the ZVS operation is also guaranteed in the optimal EPS control.

4.4 Linearization of the Optimal EPS based Control

Although the derived optimal EPS control above can achieve the minimum $I_{s,rms}$, this optimal scheme is difficult to apply in a practical on-line control scheme. The reason is mainly due to the complex relationship between D_α and D_φ (cf. Table. 4.3), which requires many square and square root mathematical operation. Therefore, it is important to simplify the optimal scheme, without sacrificing the other advantages such as minimized $I_{s,rms}$ and ZVS achievement. In the following, a linearized optimal control method is firstly introduced and then experimental results are given to validate the effectiveness of the proposed scheme.



(a)



(b)

Fig. 4.8: The RMS leakage inductance current $I_{s,rms}$ surface as a function of D_α and D_φ if the converter works in (a) Mode I, (b) Mode II for boost scenario with $k = 0.75$. [J1]

4.4.1 Linearized Optimal Control

As shown in Fig. 4.9, the optimal modulation curve (blue) can be divided into three segments depending on the D_φ range and the modulation scheme (EPS/SPS). Due to the power transfer increases with a larger D_φ (cf. Table 4.3), the separated three segments correspond to light-loading, medium-loading and heavy-loading situations. Accordingly, the coordinates $(D_\varphi,\ D_\alpha)$ of the four red points in Fig. 4.9 are used to

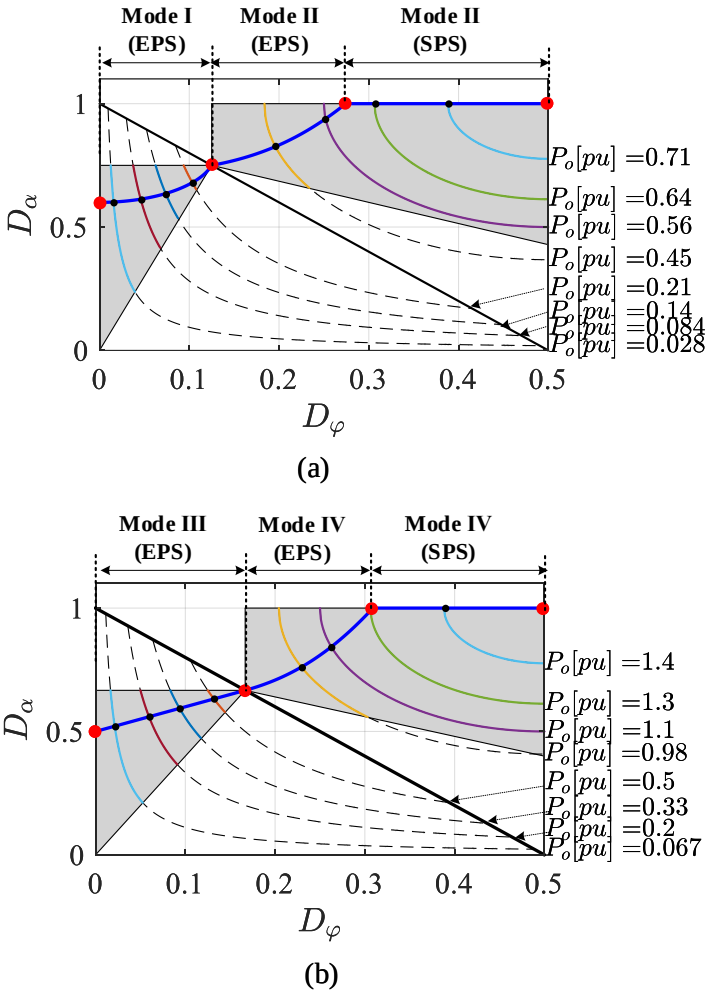


Fig. 4.9: Description of the optimal relationship $D_\alpha = f(D_\varphi)$ (denoted by the blue curve) in OMS1 when the converter works in (a) Boost scenario with $k = 0.75$ (b) Buck scenario with $k = 1.5$. Therein, the gray area is the ZVS range for each operating mode and the colored curves denote different output power levels. [J1]

identify the three loading situations, i.e.

$$\begin{cases} \left(0,\ \dfrac{k}{2-k}\right) \underset{\text{load}}{\overset{\text{Light}}{\Longrightarrow}} \left(\dfrac{1-k}{2},\ k\right) \underset{\text{load}}{\overset{\text{Medium}}{\Longrightarrow}} \left(\dfrac{k-1+\sqrt{1-k^2}}{2k},\ 1\right) \underset{\text{load}}{\overset{\text{Heavy}}{\Longrightarrow}} \left(0.5,\ 1\right) \\ \left(0,\ \dfrac{1}{2k-1}\right) \underset{\text{load}}{\overset{\text{Light}}{\Longrightarrow}} \left(\dfrac{k-1}{2k},\ \dfrac{1}{k}\right) \underset{\text{load}}{\overset{\text{Medium}}{\Longrightarrow}} \left(\dfrac{1-k+\sqrt{k^2-1}}{2},\ 1\right) \underset{\text{load}}{\overset{\text{Heavy}}{\Longrightarrow}} \left(0.5,\ 1\right) \end{cases} \tag{4.12}$$

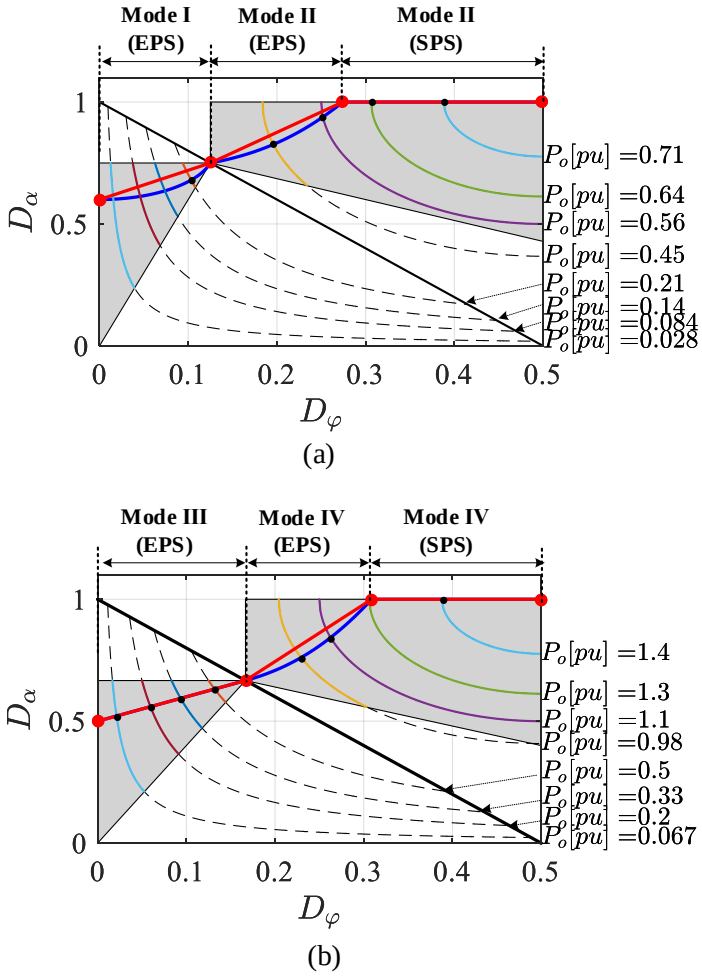


Fig. 4.10: Description of the linearized optimal relationship $D_\alpha = f(D_\varphi)$ (denoted by the red curve) in OMS4 when the converter works in (a) Boost scenario with $k = 0.75$ (b) Buck scenario with $k = 1.5$. Therein, the gray area is the ZVS range for each operating mode and the colored curves denote different output power levels. [J1]

where the upper and lower coordinates are derived from Fig. 4.9(a) and Fig. 4.9(b), corresponding to the boost scenario ($k < 1$) and buck scenario ($k > 1$), respectively.

Therefore, a linearized optimal control can be further obtained by applying a linear approximation technique to the optimal $D_{\alpha,opt}$ curves, as the red lines shown in Fig. 4.10. Combining with the coordinates in (4.12), the linearized optimal relation-

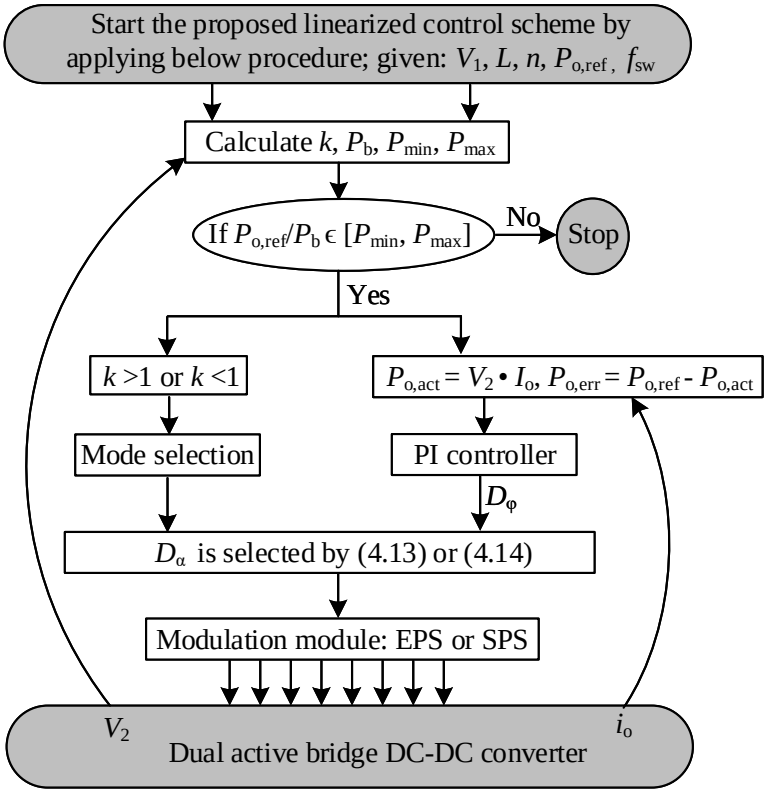


Fig. 4.11: Procedure of applying the proposed linearized control scheme to the DAB converter. [J1]

ship function between D_α and D_φ can be derived as

$$D_{\alpha,pro,boost} = \begin{cases} \frac{2k}{2-k} D_\varphi + \frac{k}{2-k}, & D_\varphi \in \left[0,\ \frac{1-k}{2}\right] \\ \frac{(2-2k^2+2\sqrt{1-k^2})}{k(1+k)} D_\varphi - \frac{(1-k)\sqrt{1-k^2}+1-k-2k^2}{k(1+k)}, & D_\varphi \in \left[\frac{1-k}{2},\ \frac{k-1+\sqrt{1-k^2}}{2k}\right] \\ 1, & D_\varphi \in \left[\frac{k-1+\sqrt{1-k^2}}{2k},\ 0.5\right] \end{cases} \tag{4.13}$$

$$D_{\alpha,pro,buck} = \begin{cases} \frac{2}{2k-1} D_\varphi + \frac{1}{2k-1}, & D_\varphi \in \left[0,\ \frac{k-1}{2k}\right] \\ \frac{2k\sqrt{k^2-1}+2k^2-2}{k+1} D_\varphi - \frac{(k-1)\sqrt{k^2-1}+k^2-k-2}{k+1}, & D_\varphi \in \left[\frac{k-1}{2k},\ \frac{1-k+\sqrt{k^2-1}}{2}\right] \\ 1, & D_\varphi \in \left[\frac{1-k+\sqrt{k^2-1}}{2},\ 0.5\right] \end{cases} \tag{4.14}$$

where (4.13) and (4.14) are the linearized results for the boost scenario (cf. Fig. 4.10(a))

and buck scenario (cf. Fig. 4.10(b)), respectively. Noting that there are also complex quare root operations in the coefficients of (4.13) and (4.14), but they are all based on the voltage ratio k and these coefficients can be taken as a constant if the input and output dc voltages are known. For example, if $k = 0.75$ and $k = 1.5$ are given for the respective boost and buck scenarios, the specific linearized results are

$$D_{\alpha,pro,boost} = \begin{cases} 1.2D_\varphi + 0.6, & D_\varphi \in [0,\ 0.13] \\ 1.67D_\varphi + 0.54, & D_\varphi \in [0.13,\ 0.27] \\ 1, & D_\varphi \in [0.27,\ 0.5] \end{cases} \tag{4.15}$$

$$D_{\alpha,pro,buck} = \begin{cases} D_\varphi + 0.5, & D_\varphi \in [0,\ 0.17] \\ 2.34D_\varphi + 0.28, & D_\varphi \in [0.17,\ 0.31] \\ 1, & D_\varphi \in [0.31,\ 0.5] \end{cases} \tag{4.16}$$

The procedure of applying the linearized control scheme to the DAB converter is presented in Fig. 4.11. Firstly, the voltage ratio k, the base power P_b and the minimum power P_{min} and maximum power P_{max} can be calculated according to the given converter parameters. If the given power $P_{o,ref}$ is not within the range of $[P_{min},\ P_{max}]$, the procedure stops since the given power exceeds the available power range of the DAB converter. If a proper $P_{o,ref}$ is given, the error between the given power and the measured output power $P_{o,act}$ is regulated by a PI controller. Simultaneously, the operation mode (i.e. Mode I, II, III, IV) is conformed by the voltage ratio k and the given power $P_{o,ref}$. Then the value of D_{alpha} can be calculated utilizing the derived linear expression (4.13) or (4.14). Based on D_φ and D_α, the relevant modulation scheme (EPS or SPS) is applied to the DAB converter by generating corresponding driving signals.

4.4.2 Control Schemes Comparison

Seen from the linearized optimal lines (red) and the optimal curves (blue) in Fig. 4.10, there are slight mismatch between the lines and curves. This means that the effect of the approximating scheme on $I_{s,rms,opt}$ is not as good as the optimal scheme. In order to evaluate the deviation from the minimum $I_{s,rms}$ with the linearized control scheme, the relative errors $i_{err,pro}$ expressed by

$$i_{err,pro} = \frac{|I_{s,rms,pro} - I_{s,rms,opt}|}{I_{s,rms,opt}} \cdot 100\% \tag{4.17}$$

for different voltage ratios and output powers are shown in Fig. 4.12.

As comparison, the relative errors $i_{err,SPS}$ between the RMS current with SPS modulation (denoted by $I_{s,rms,sps}$) and the minimum $I_{s,rms,opt}$ are calculated and depicted in Fig. 4.12.

$$i_{err,SPS} = \frac{|I_{s,rms,SPS} - I_{s,rms,opt}|}{I_{s,rms,opt}} \cdot 100\% \tag{4.18}$$

In Fig. 4.12, the x-axis power labels $P_i (i = 1..15)$ are calculated by

$$P_i = \begin{cases} 0.2 \cdot i \cdot P_5, & i = 1..5 \\ P_5 + 0.2 \cdot (i-5) \cdot (P_{10} - P_5), & i = 6..10 \\ P_{10} + 0.2 \cdot (i-10) \cdot (P_{15} - P_{10}), & i = 11..15 \end{cases} \tag{4.19}$$

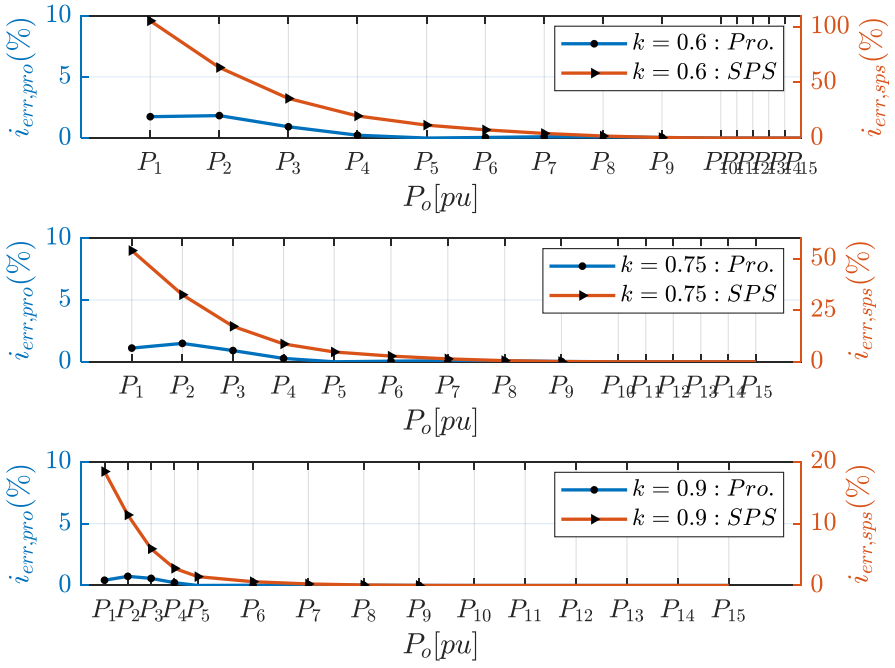


Fig. 4.12: At different power levels $P_1 \sim P_{15}$, relative errors between (defined by (4.17) and (4.18)) the calculated RMS leakage inductance currents using the optimal control scheme and the proposed linearized control scheme. [J1]

with

$$P_5 = 2k^2(1-k), \quad P_{10} = \frac{2(k^2 - 1 + \sqrt{1-k^2})}{k}, \quad P_{15} = k \tag{4.20}$$

In detail, P_5, P_{10} and P_{15} are the output powers at the three boundary points, i.e. $[(1-k)/2, k]$, $[(k-1+\sqrt{1-k^2})/(2k), 1]$, $[0.5, 1]$.

By comparing $i_{err,sps}$ and $i_{err,pro}$ in Fig. 4.12, it can be concluded that the proposed linear control scheme can achieve lower RMS current than SPS, especially in light and medium loading situations. Besides, the small relative errors $i_{err,pro}$ (less than 2%) indicate that although the proposed linear control scheme might lead to a slightly larger RMS current than the optimal control, it is worth employing the proposed linear control scheme in terms of an easy on-line calculation.

4.4.3 Experimental Validation

The same experimental platform shown in Fig. 2.4 is utilized to validate the proposed linear control scheme, and the system parameters of the DAB converter are as listed in Table 4.4. In order to fully evaluate the proposed control scheme, the converter is operated at three different power levels (i.e. light-, medium- and heavy-load) for either boost or buck voltage scenario. Moreover, another group of experiments using

Table 4.4: System Specifications [J1]

Parameters	Description	Value
P	Power rating	1.5 kW
$n:1$	Turns ratio of the transformer	3.5 : 1
f_{sw}	Switching frequency	60 kHz
T_{dead}	Dead time	400 ns
L_s	Series inductor	36.2 μH
L_{trp}	Primary-side leakage inductance	4.5 μH
L_{trs}	Secondary-side leakage inductance	372.5 nH
C_1	Primary DC capacitor	0.78 mF
C_2	Secondary DC capacitor	1.5 mF

the conventional EPS modulation are conducted, where the ZVS is also achieved to cancel out the influence of the switching losses. Thus, the effect of the proposed linear control on the conduction losses reduction can be obtained by comparing the RMS leakage inductance current and the system efficiency.

In Mode I (light-load, boost scenario), the working waveforms at steady state are illustrated in Fig. 4.13, where Fig. 4.13(a) shows the waveforms without adopting any optimized modulation and Fig. 4.13(b) with the proposed linear control scheme. In both working situations, the output power is 190 W. v_p, v_s are the respective terminal voltages of the primary and secondary full-bridges, and i_p, i_s are the primary secondary winding currents, respectively. By importing the sampled data from the oscilloscope to MATLAB, the RMS value of the secondary current can be calculated, as marked by $I_{s,rms}$ in Fig. 4.13. It can be seen that the RMS current $I_{s,rms}$ is lower in Fig. 4.13(b) than that in Fig. 4.13(a), and this indirectly proves that the proposed linear control scheme can effectively reduce the conduction losses. Meanwhile, the converter efficiency is increased from 92.5% to 95% resulting from the losses reduction.

Besides, the gate driving signal $v_{GS,S7}$ and the drain-source voltage $v_{DS,S7}$ of the power device S_7 are illustrated in Fig. 4.13(c), where the operating condition is the same as Fig. 4.13(b). At the turn-on instant of the S_7, which is also the positive rising instant of v_s, the drain-source voltage has decreased to zero before the gate-source voltage reaches a high level. This implies that ZVS turn-on is achieved for S_7. Similarly, the ZVS of the other power devices can also be validated by this method, which indicates that the proposed linear control scheme can guarantee the ZVS realization.

In Mode II (medium- and heavy-load, boost scenario), due to that the modulation scheme is different depending on the loading situation (cf. (4.12)), two power levels are applied to the DAB converter. The working waveforms with $P_o = 430\ W$ are shown in Fig. 4.14 and $P_o = 700\ W$ in Fig. 4.15. Similar to Fig. 4.13, $I_{s,rms}$ is decreased

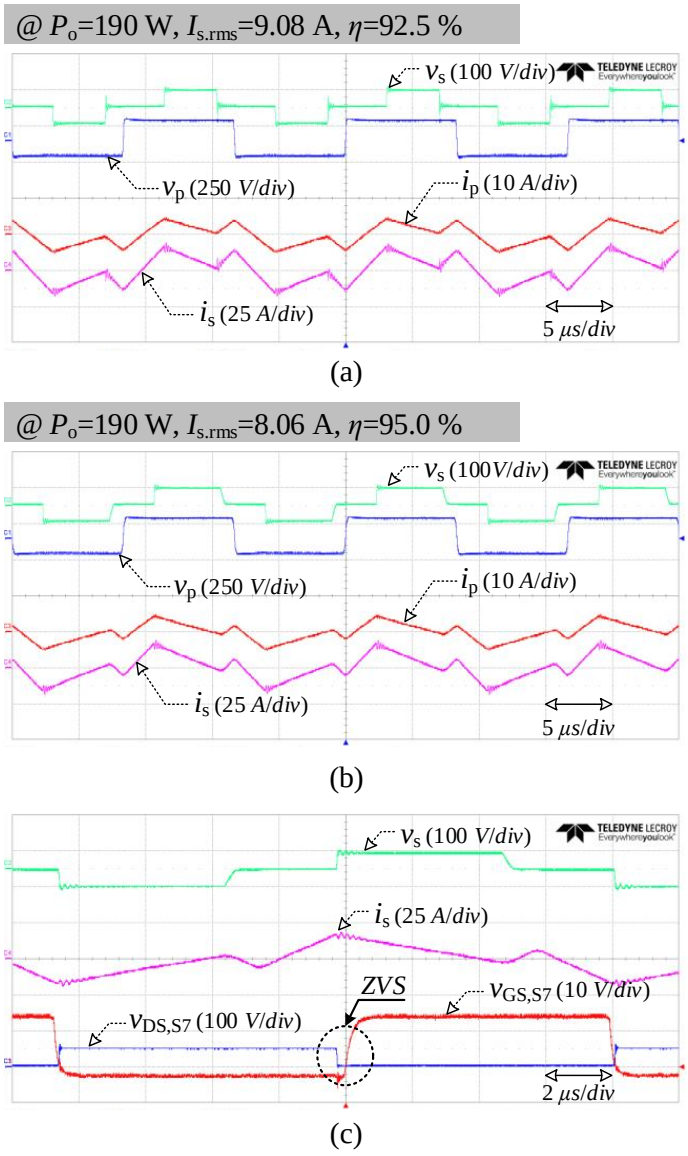


Fig. 4.13: Operating waveforms in Mode I (EPS) where $V_1 = 120\ V$, $V_2 = 46\ V$, $k = 0.75$ (a) without optimization (b) with proposed linearized control scheme (c) ZVS realization of the proposed control scheme. [J1]

with the proposed linear control scheme and consequently, the power conversion efficiency is improved by comparing Fig. 4.14(b), Fig. 4.15(b) with Fig. 4.14(a), Fig. 4.15(a). In terms of the ZVS of S_7 in Fig. 4.14(c) and Fig. 4.15(c), although some

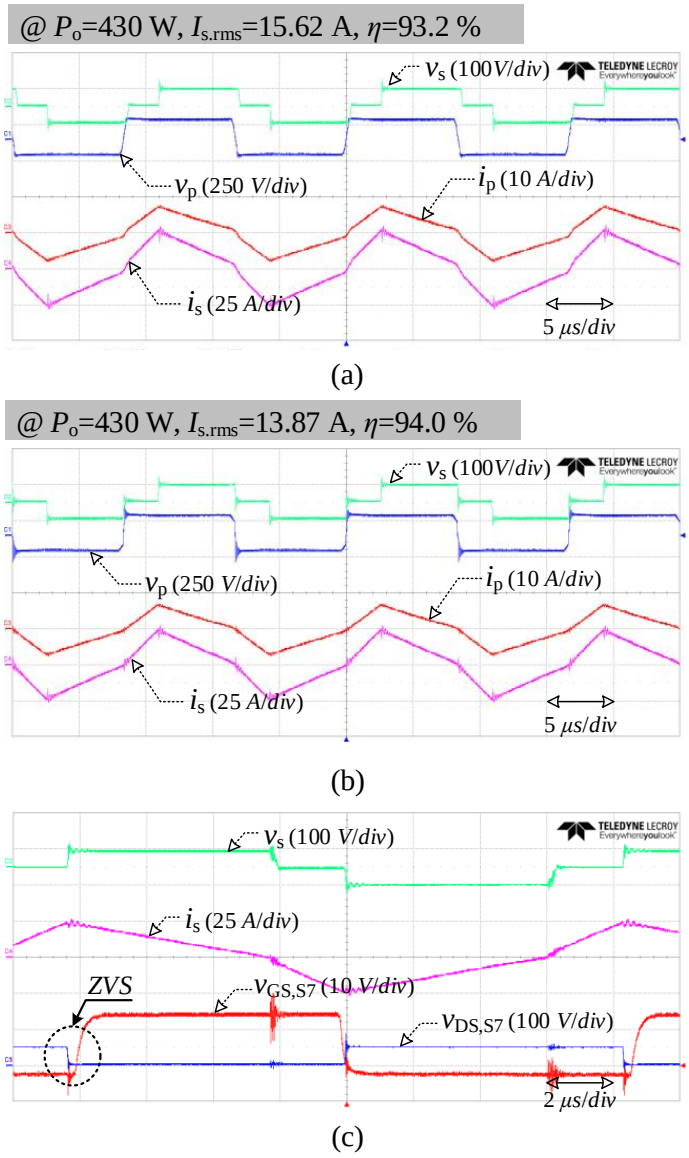


Fig. 4.14: Operating waveforms in Mode II (EPS) where $V_1 = 120\ V$, $V_2 = 46\ V$, $k = 0.75$ (a) without optimization (b) with proposed linearized control scheme (c) ZVS realization of the proposed control scheme. [J1]

oscillations occur at the turn-on instant of S_7, the drain-source voltage is clamped at zero before the driving signal becomes high. This reveals that ZVS is still guaranteed ín medium- and heavy-load for boost scenarios.

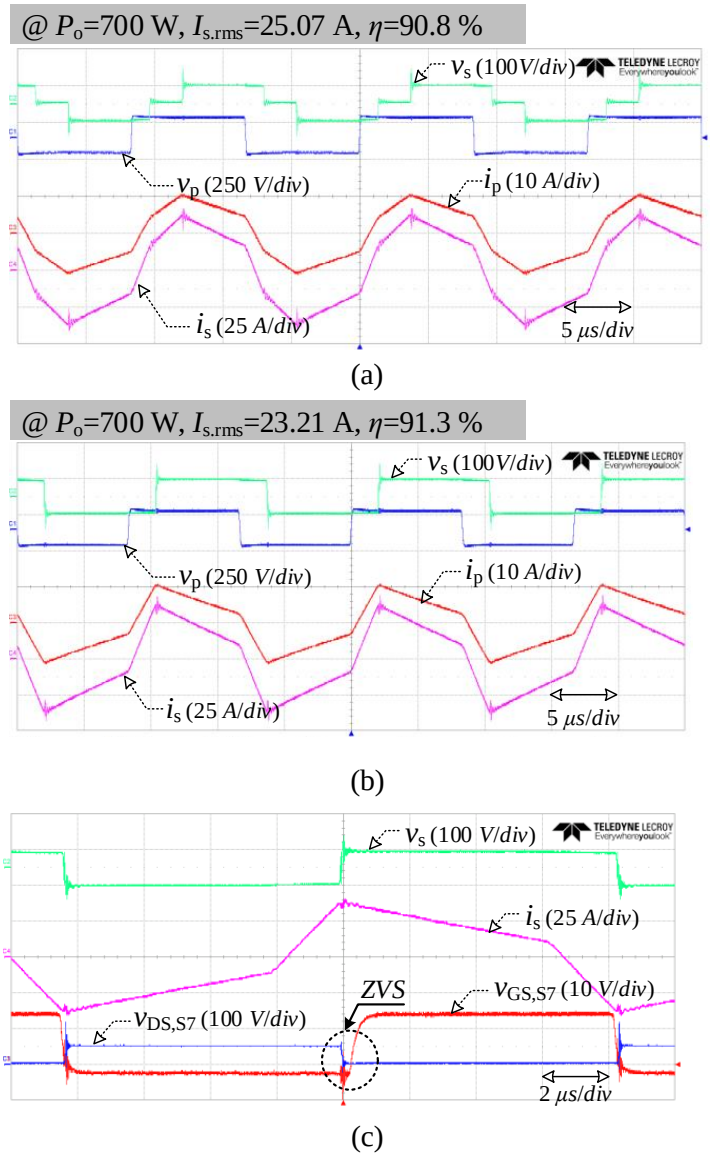


Fig. 4.15: Operating waveforms in Mode II (SPS) where $V_1 = 120\ V$, $V_2 = 46\ V$, $k = 0.75$ (a) without optimization (b) with proposed linearized control scheme (c) ZVS realization of the proposed control scheme. [J1]

With respect to the buck scenarios, steady state working waveforms are shown in Fig. 4.16 $\sim$ Fig. 4.18 with different loading situations, corresponding to Mode III or Mode IV. Similar conclusions concerning the conduction losses reduction, effi-

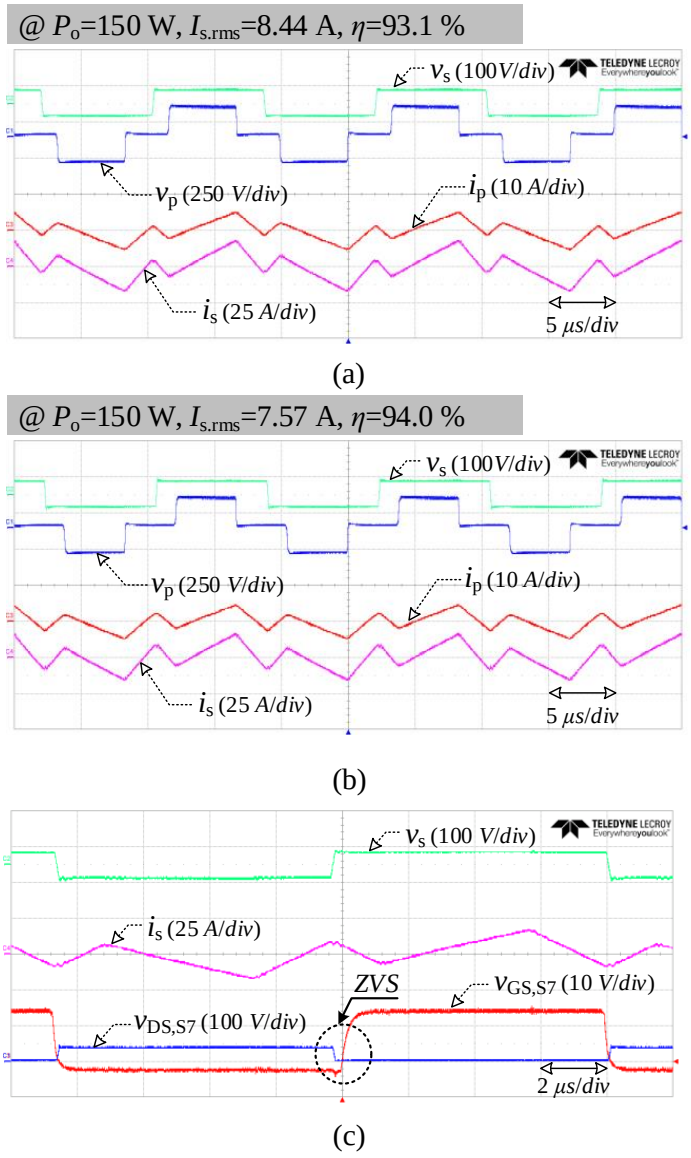


Fig. 4.16: Operating waveforms in Mode III (EPS) where $V_1 = 190\ V$, $V_2 = 36\ V$, $k = 1.5$ (a) without optimization (b) with proposed linearized control scheme (c) ZVS realization of the proposed control scheme. [J1]

ciency improvement and ZVS achievement can be obtained, which validates that the proposed linear control scheme is also applicable to buck scenarios.

As indicated in (4.13) and (4.14), the proposed linear control scheme employs EPS

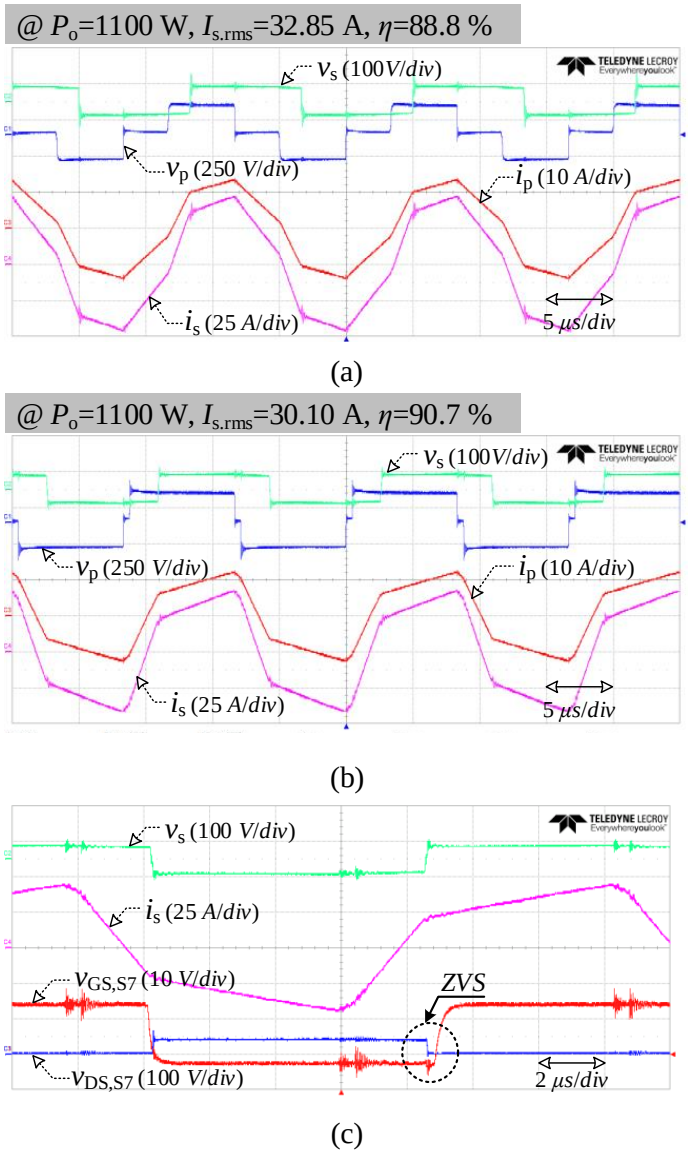


Fig. 4.17: Operating waveforms in Mode IV (EPS) where $V_1 = 190\ V$, $V_2 = 36\ V$, $k = 1.5$ (a) without optimization (b) with proposed linearized control scheme (c) ZVS realization of the proposed control scheme. [J1]

in light load and SPS in heavy load. In order to validate the dynamic performance of the proposed control scheme, the output power of DAB converter is switched between the light-load 150 W and the heavy-load 700 W. The transient waveforms are shown in

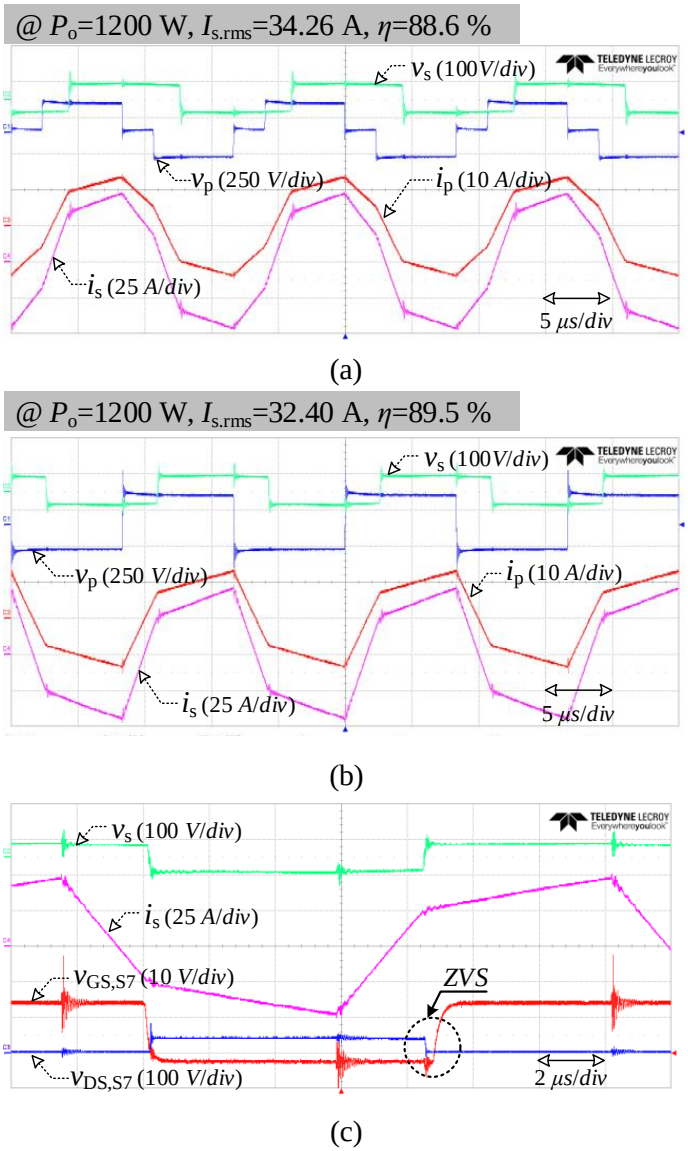


Fig. 4.18: Operating waveforms in Mode IV (SPS) where $V_1 = 190\ V$, $V_2 = 36\ V$, $k = 1.5$ (a) without optimization (b) with proposed linearized control scheme (c) ZVS realization of the proposed control scheme. [J1]

Fig. 4.19, where V_2 is the output voltage (kept constant), i_o is the output dc current and i_s is the secondary side high-frequency ac current. It can be seen that the proposed control scheme can smoothly switch the DAB converter between different loading

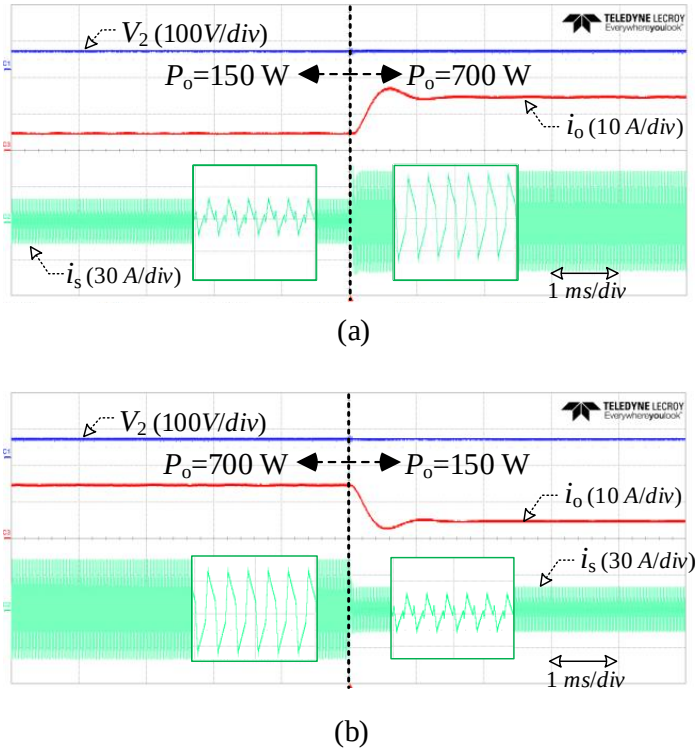


Fig. 4.19: Dynamic response with the output power (a) increased from 150 W to 700 W (b) decreased from 700 W to 150 W in boost scenario with $V_1 = 120\ V$, $V_2 = 46\ V$. [J1]

situations and applying the proper modulation scheme to the converter.

Furthermore, the converter efficiency is measured by operating the converter with various power levels, different voltage ratios and modulation schemes, and the results are shown in Fig. 4.20. Fig. 4.20(a) and Fig. 4.20(b) correspond to the boost scenario ($k = 0.9$) and the buck scenario ($k = 1.2$), respectively. In each figure, the measured efficiency using the proposed linear control scheme, the conventional extended phase-shift modulation without any optimization and the earliest single phase-shift modulation are denoted by the red, blue and black curves, respectively. It can be seen that the proposed linear control scheme has a higher efficiency in both buck and boost scenarios. In light load, due to the ZVS failure in SPS (the other two schemes Pro and EPS can maintain ZVS), the induced switching losses result in much lower efficiency. In heavy load, the proposed linear control transfer to single phase shift modulation scheme and thus the efficiency curves of Pro and SPS are overlapped in the higher power range.

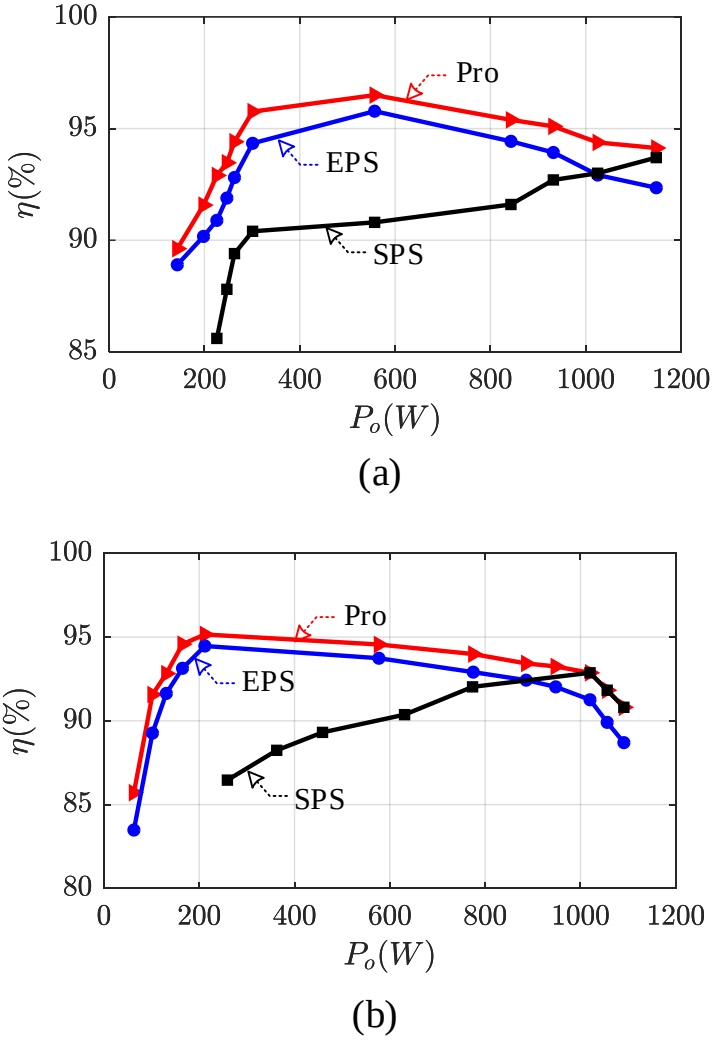


Fig. 4.20: Measured efficiency curves for different output power levels, where the red curve, blue curve and black curve denote the converter efficiencies with linear modulation scheme, without any optimization and with SPS, respectively, in (a) boost operation with $V_1 = 190\ V$, $V_2 = 60\ V$, $k = 0.9$ (b) buck scenario with $V_1 = 190\ V$, $V_2 = 45\ V$, $k = 1.2$. [J1]

4.5 Summary

In order to simplify the optimized DAB converter control on reducing the conduction losses, an extended-phase-shift based linearized control scheme is introduced in this chapter. Without sacrificing the ZVS over the whole operating range and the maxi-

mum power transfer as the single-phase-shift modulation, the optimal control is firstly derived, which can achieve the minimum leakage inductance current. On this basis, the control procedure is further simplified and a linear control scheme is proposed. As a result, it becomes easier for on-line control and meanwhile a quasi-minimum leakage inductance current is achieved.

Chapter 5

Active Thermal Control of DAB for Reliability Improvement

5.1 Background

As the power electronic converters and systems have recently been substantially developed in many applications from energy generation to consumption [101–103], the reliability is becoming an important issue, and much research has been devoted to the power devices and capacitors as well as the system analysis [104–106]. Focusing on the power device reliability research, many failure mechanisms are related to the high average temperature and temperature swing [104, 106, 107]. From the perspective of long-term running, the temperature swing most often plays a more important role in the wear-out failures. The main root cause is the inconsonant coefficients of thermal expansion among different materials inside a package, and a large temperature swing will repeatedly heat and cool the power device until bond-wire lift-off or solder crack occurs.

From the viewpoint of transient or short-term operation, the over temperature is more likely to cause a considerable damage to the power device, such as chip solder melting and large area solder joint melting between the substrate and the base plate in a package [104]. Besides, if the power device is continuously operated at a high ambient temperature, such as inside a electric vehicle in hot weather [108–110], the strain and related stress in the solder will increase a lot and ultimately break [106].

Rather than in the design phase, where the reliability can be improved by proper circuit design and component selection [111, 112], an approach to improve the converter and system reliability by actively controlling the thermal stresses among power devices is proposed. As shown in Fig. 5.1, there are different optimization targets in active thermal control, e.g. switching loss reduction [113, 114], conduction loss reduction [115, 116], reactive power control [101, 117, 118] and active power control

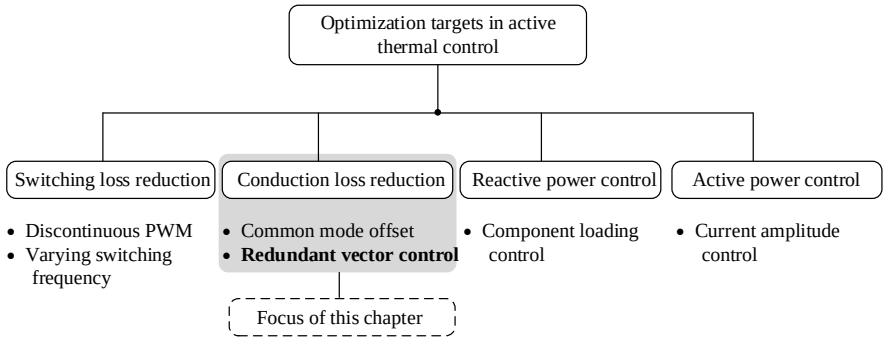


Fig. 5.1: Active thermal control methods with different optimization targets.

[119, 120]. Therein, reducing the conduction losses to achieve an improved reliability of the DAB converter is the focus of this chapter.

5.2 Impacts of On-state Resistance Drift

As shown in Fig. 4.3, if ZVS is achieved in the DAB converter, the conduction losses become the dominating part of the total power losses, especially in medium- and heavy-loading situations. However, these conduction losses might unevenly be distributed on the power devices due to the slight parameter drifts among a large number of power device products. For example, the value of the on-state resistance $R_{DS,on}$ usually has a minimum value and a maximum value in the product data sheet. If the power device is operating in a converter, $R_{DS,on}$ might even vary in a wide range depending on the gate-source voltage, the drain current and particularly on the junction temperature. On the other hand, the thermal dissipation of each power device could be different due to the imperfect design of the circuit board. Consequently, the thermal loadings of power devices could vary widely, and the most stressed power device will limit the lifetime and power rating of the DAB converter.

For an improved converter reliability, the thermal loading of the most stressed power device should be reduced. This can be achieved by reconfiguring the switching sequence and the duty cycles of the power devices in operation. Thus, the current flowing path among the power devices can be rerouted and the generated losses by the most stressed power device can be suppressed, leading to a decreased junction temperature and a longer lifetime.

In the conventional modulation strategy, the power devices in a DAB converter are switched with a fixed 50% duty cycle and the phase-shift angles among different switching signals are utilized to control the power transfer. As discussed in last chapter, the optimized EPS modulation method is applied to the DAB circuit as shown in Fig. 5.2, and correlated working waveforms are shown in Fig. 5.3(a). Therein, D_φ is the phase-shift between the primary voltage v_p and the secondary voltage v_s, and D_α is the duty cycle of v_s.

Based on the derivation in last chapter, the conduction losses of each switch in the

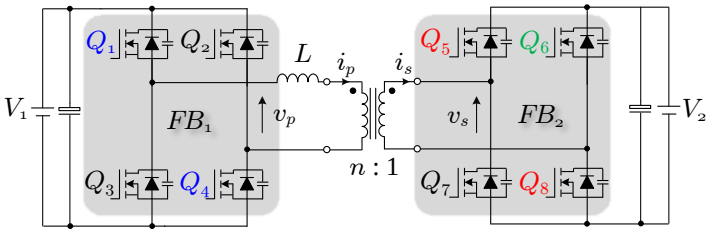


Fig. 5.2: Circuit topology of the DAB converter.

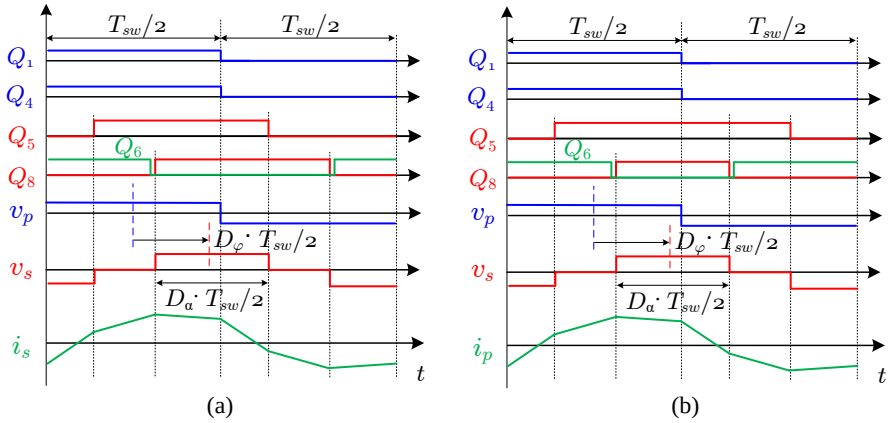


Fig. 5.3: Working waveforms with (a) conventional extended-phase-shift modulation (b) modified extended-phase-shift modulation.

secondary-side can be calculated by

$$P_{cond} = \frac{R_{DSons}}{4} \cdot \left(\frac{I_{s,rms}}{\sqrt{2}}\right)^2 \tag{5.1}$$

where R_{DSons} is the on-state resistance of the power device and $I_{s,rms}$ is the leakage inductance current referred to the secondary side. Note that each switch in the primary side (i.e. $Q_1 \sim Q_4$ in Fig. 5.2) is one IPW65R080CFD, and each in the secondary side (i.e. $Q_5 \sim Q_8$ in Fig. 5.2) is composed of two paralleled IPP110N20N3G to reduce the current stress. Detailed information can be found in Table 4.1.

Seen from (5.1), the conduction losses of each power device would be identical if R_{DSons} and $I_{s,rms}$ are kept constant among $Q_5 \sim Q_8$. However, due to the parameter drift in a large number of power device products, the values of R_{DSons} are slightly varied even at the same junction temperature (denoted by T_j). For instance, as stated in the datasheet of IPP110N20N3G, the on-state resistance has a typical value of 9.9 $m\Omega$ and a maximum value of 11 $m\Omega$ at $T_j = 25\,^oC$. In addition, the on-state resistance is increased with a higher junction temperature, as shown in Fig. 5.4. This will cause a potential larger parameter drift in transient operating states because of the positive

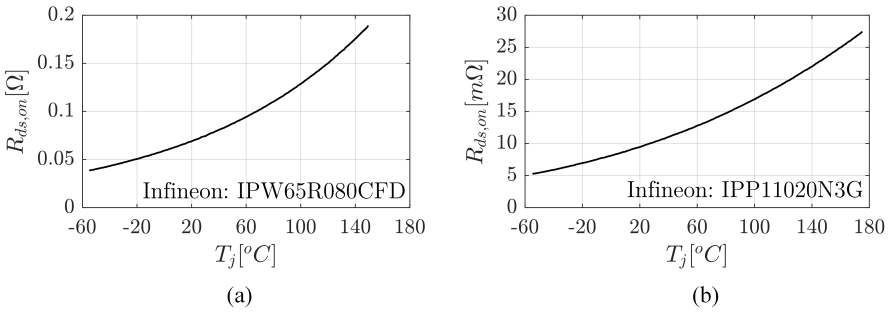


Fig. 5.4: Datasheet profiles of the on-state resistance $R_{ds,on}$ varying with the junction temperature T_j for the utilized (a) IPW65R080CFD (b) IPP110N20N3G in the built DAB setup.

Table 5.1: Simulation Parameters of the DAB Converter

Parameters	Description	Value
V_1	Input dc voltage	400 V
V_2	Output dc voltage	150 V
$n:1$	Turns ratio of the transformer	3.5 : 1
f_{sw}	Switching frequency	60 kHz
T_{dead}	Dead time	400 ns
L	Leakage inductance	45 μH
C_{thh}	Thermal capacitance of the heatsink	0.1 mJ/K
R_{thh}	Thermal resistance of the heatsink	0.5 K/W

correlation between R_{DSons} and T_j. Besides, due to the existence of deadtime, the RMS values of the drain currents for the power devices in one leg are also not exactly the same. Therefore, the generated conduction losses of each power device might differ a lot from each other, which will further lead to different thermal stresses.

By assuming a 2 $m\Omega$ difference of $R_{ds,on}$ among the power devices at lower junction temperatures, the conduction power losses of each IPP110N20N3G in Q_5 and Q_8 can be obtained, as shown in Fig. 5.5(a). In this case, there are $T_{j,Q5} = 40\ ^oC$ and $T_{j,Q8} = 63\ ^oC$, leading to $R_{ds,on,Q5} = 11\ m\Omega$ and $R_{ds,on,Q8} = 13\ m\Omega$. At a higher junction temperature, the $R_{ds,on}$ difference might increase. As an example of $T_{j,Q5} = 125\ ^oC$ and $T_{j,Q8} = 160\ ^oC$, the losses curves with $R_{ds,on,Q5} = 20\ m\Omega$ and $R_{ds,on,Q8} = 25\ m\Omega$ are also depicted in Fig. 5.5(a). Relevant converter parameters for calculating the conduction losses P_{cond} are listed in Table 5.1.

Seen from Fig. 5.5(a), Q_8 would be the most stressed power device with a higher

on-state resistance. In order to achieve a thermal balance between Q_5 and Q_8, a modified EPS modulation method as shown in Fig. 5.3(b) can be utilized to reduce the conduction power losses of Q_8. Compared to the conventional EPS modulation in Fig. 5.3(a), the duty cycle of Q_8 is reduced while the waveforms of v_p and v_s are kept unchanged. In other words, the modified EPS modulation has no effect on the control variables D_φ and D_α, thus the other converter performances such as the ZVS range and the power transfer capability do not have to be sacrificed. However, in order to maintain a constant shape of v_s, the duty cycle of Q_5 is increased in Fig. 5.3(b), which might lead to newly unbalanced thermal stresses of Q_5 and Q_8.

Based on the working waveforms in Fig. 5.3(b), the conduction losses of each IPP110N20N3G in Q_5 and Q_8 can be derived as

$$\begin{cases} P_{cond,Q5} = \dfrac{R_{DSons}}{4} \cdot \left(I_{s,rms} \sqrt{1 - \dfrac{D_\alpha}{2}} \right)^2 \\ P_{cond,Q8} = \dfrac{R_{DSons}}{4} \cdot \left(I_{s,rms} \sqrt{\dfrac{D_\alpha}{2}} \right)^2 \end{cases} \tag{5.2}$$

Similarly, the varying curves of $P_{cond,Q5}$ and $P_{cond,Q8}$ can be obtained according to (5.2), as shown in Fig. 5.5(b). It can be seen that by applying the modified EPS modulation, the conduction losses of Q_5 are larger than that of Q_8 with a small D_φ. With the increase of D_φ, the modified EPS is unable to cancel the effect of $R_{ds,on}$ drift and thereby $P_{cond,Q8}$ becomes again larger than $P_{cond,Q5}$.

5.3 Active Thermal Control with Hybrid EPS

As discussed above, due to the on-state resistance drift in practice, thermal unbalance always occur by only using either conventional or modified EPS modulation. Thus it is natural to consider combining together these two EPS modulation methods as shown in Fig. 5.3. Since the conventional EPS would lead to a higher $T_{j,Q8}$ than $T_{j,Q5}$ and the modified EPS can decrease the difference between $T_{j,Q8}$ and $T_{j,Q5}$, a hysteresis control can be employed to balance the thermal stresses on Q_5 and Q_8.

The schematic diagram of the converter control is as shown in Fig. 5.6, including electric and thermal controlling. In the electric control, the output current i_2 is averaged through a digital/physical low pass filter and then it is multiplied by the output dc voltage V_2 to obtain the actual output power P_o. A PI controller is utilized to regulate the output power, and the regulated phase-shift D_φ is input to the linear control block (cf. (4.13) in last chapter) to generate the optimal D_α. Considering the varying battery voltage in an EV, the input and output dc voltages are sampled in real-time, and the voltage ratio V_1/nV_2 is imported to the linear control block.

Regarding the thermal control, the hybrid EPS modulation including the conventional (Conv.) and the modified (Modi.) EPS modulation is employed. The junction temperatures of Q_5 ($T_{j,Q5}$) and Q_8 ($T_{j,Q8}$) are firstly measured, which can be achieved through an electro-thermal model [121–123], a junction temperature estimator [107, 124, 125], or it can be directly measured with the thermal couple, optic fiber or infrared camera. Then the sampled $T_{j,Q5}$ and $T_{j,Q8}$ are compared. If the error between $T_{j,Q5}$ and $T_{j,Q8}$ is larger than 0.2^oC, the conventional EPS modulation is

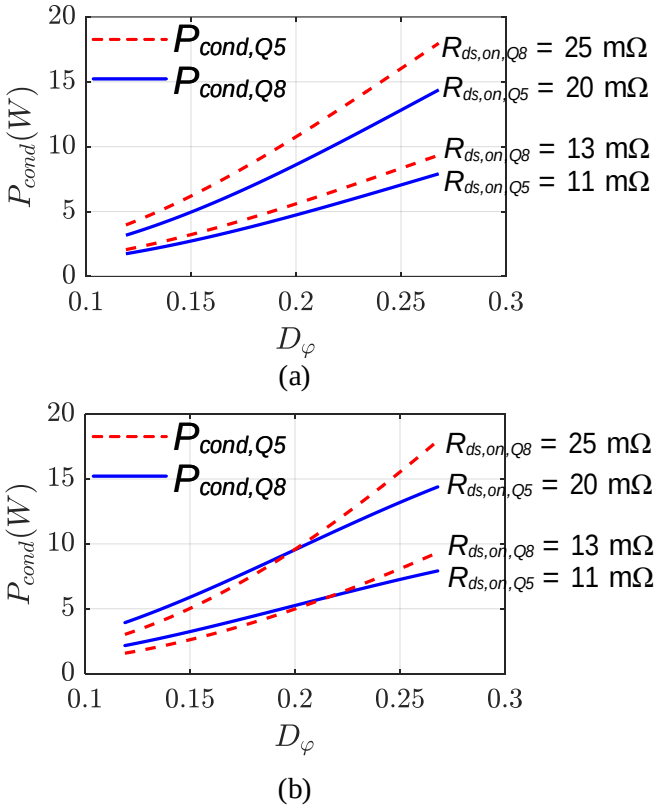


Fig. 5.5: Conduction losses of each IPP110N20N3G in Q_5 and Q_8 with different on-state resistances using (a) conventional extended-phase-shift modulation (cf. Fig. 5.3(a)) (b) modified extended-phase-shift modulation (cf. Fig. 5.3(b)).

applied with a higher $T_{j,Q5}$, or else the modified EPS modulation is adopted with a higher $T_{j,Q8}$. Then together with the regulated D_φ and D_α from the electric control, the switching signals can be generated.

In order to verify the effectiveness of the thermal control, the simulation results using the converter parameters listed in Table 5.1 are shown in Fig. 5.7. The converter is transferred from the conventional EPS to the modified EPS at $t = 0.7\ ms$, and the active thermal control (cf. Fig. 5.6) using hybrid EPS modulation is enabled at $t = 1.5\ ms$. It can be seen that the steady junction temperature of Q_8 is larger than that of Q_5 due to a larger on-state resistance of Q_8 at the beginning $t \in [0,\ 0.7\ ms]$. If only the modified EPS modulation is applied within $t \in [0.7\ ms,\ 1.5\ ms]$, $T_{j,Q8}$ becomes smaller than $T_{j,Q5}$ as a result from the reduced conduction time of Q_8 in one switching period. After combining the two EPS modulations and applying the hysteresis control during $t \in [1.5\ ms,\ 2\ ms]$, a thermal loading balance between Q_5 and Q_8 is achieved, which is reflected by the equal junction temperatures of Q_5 and Q_8.

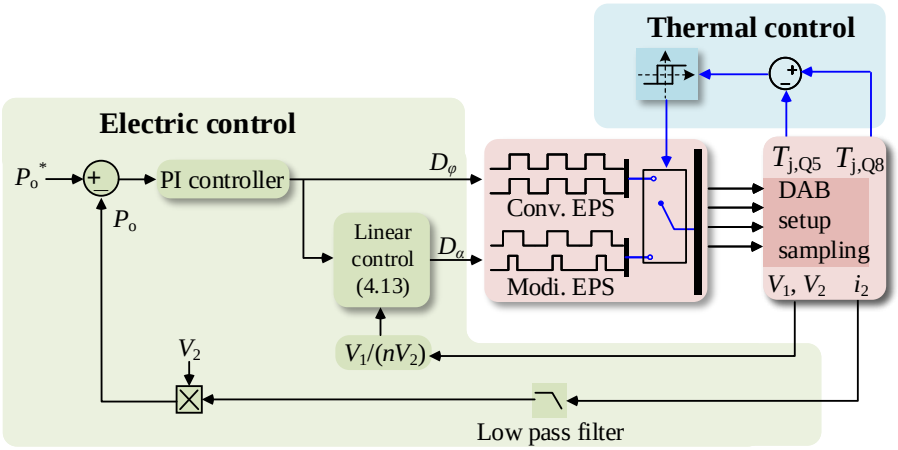


Fig. 5.6: Schematic diagram of the active thermal control of Q_5 and Q_8 using hysteresis comparison.

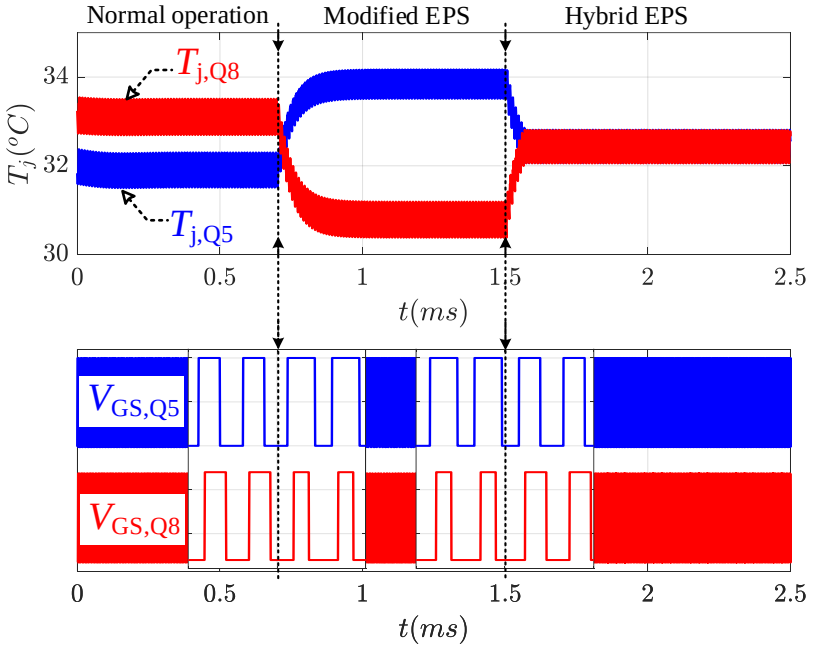


Fig. 5.7: Simulated results of the active thermal control using hybrid EPS modulation with $R_{ds,on,Q5} = 11\ m\Omega$ and $R_{ds,on,Q8} = 13\ m\Omega$.

Table 5.2: Experimental Parameters of the DAB Converter

Parameters	Description	Value
V_1	Input dc voltage	100 V
V_2	Output dc voltage	30 V
D_α	Duty cycle of v_s	0.72
f_{sw}	Switching frequency	60 kHz
T_{dead}	Dead time	400 ns
L	Leakage inductance	45 μH

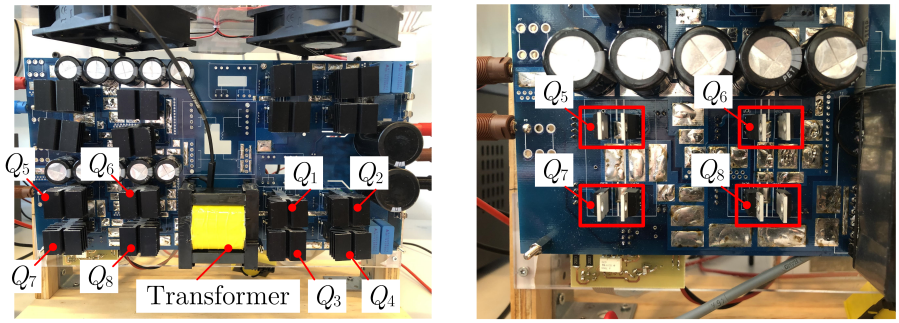


Fig. 5.8: The built DAB setup (a) front view of whole circuit board (b) amplified view of the power devices $Q_5 \sim Q_8$.

5.4 Experimental Validation

In order to verify the effect of hybrid EPS modulation on the thermal control, the operating parameters listed in Table 5.2 are applied to the built DAB setup as shown in Fig. 5.8. By switching the converter between the conventional and the modified EPS modulation, the driving signals of $V_{GS,Q1}$, $V_{GS,Q5}$ and $V_{GS,Q8}$ are as shown in Fig. 5.9. Therein, the signal V_{step} is used to capture the modulation method transition. It can be seen that the driving signals can smoothly shift between the two modulation methods.

Operating the converter with an output power of 420 W, the steady-state working waveforms are shown in Fig. 5.10(a) and Fig. 5.10(b), utilizing the conventional and the modified EPS modulation, respectively. Seen from the waveforms of v_p, v_s and i_s in Fig. 5.10, they are kept unchanged and this is consistent with the previous analysis and simulation.

As the secondary-side power devices have a larger current than the primary-side ones (caused by the transformer turns ratio of 3.5 : 1 from primary to secondary), $Q_5 \sim Q_8$ have a larger thermal stress than $Q_1 \sim Q_4$ and they are thus selected

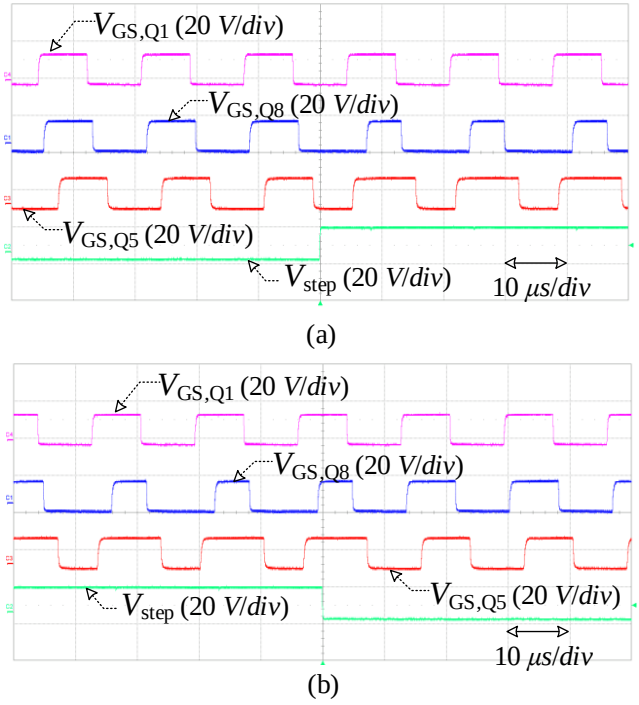


Fig. 5.9: Driving signals when the converter transfers (a) from conventional EPS modulation to modified EPS modulation (b) from modified EPS modulation to conventional EPS modulation, both with $D_\varphi = 0.31$.

as the research targets. The heatsinks of $Q_5 \sim Q_8$ in Fig. 5.8(a) are removed (cf. Fig. 5.8(b)) for the convenience of measuring the case temperature with a infrared camera. Note that in order to avoid possible unbalanced external thermal dissipation, the fan for cooling down the devices is ceased during operation, and thus the power devices will be continuously heated up. In order to operate the power devices within a safe temperature range and meanwhile to fairly compare the effects of different EPS modulation methods, initial case temperatures are kept as identical as possible and the operating time is set as 2 minutes for each experiment. The whole temperature changing process in the 2 minutes is recorded in a video. Then the initial frame and final frame are extracted from the video to obtain the start and end case temperatures.

Three groups of experiments are conducted with different output power levels. Each group includes two experiments, i.e. the conventional modulation method without active thermal control and the hybrid modulation method with active thermal control. It should be noted that in the active thermal control experiments, the conventional method is operated with 8 seconds followed by another 4 seconds of the modified EPS modulation, and then this total 12-seconds operating period is repeated until the 2 minutes limitation.

In the first group, the converter is operated with an output power of 320 W, and

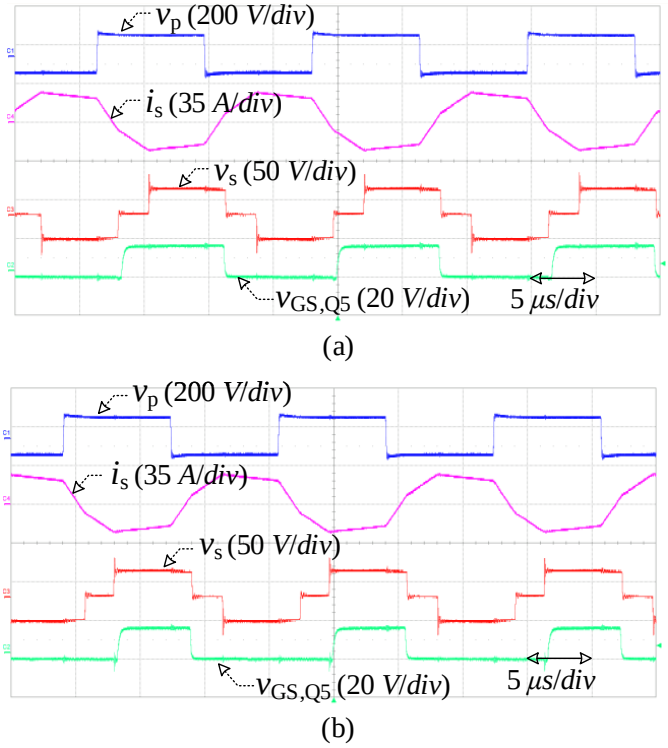
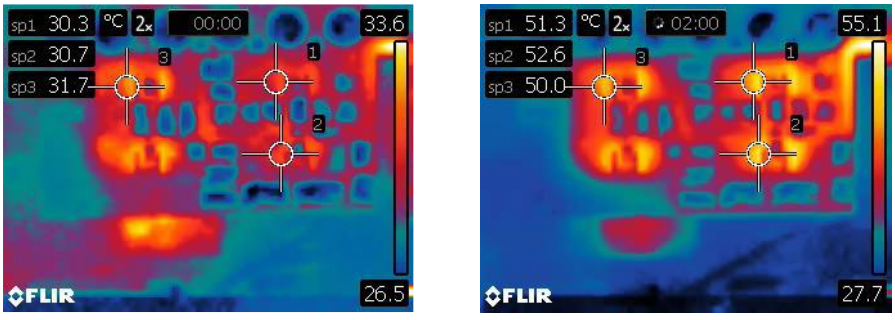


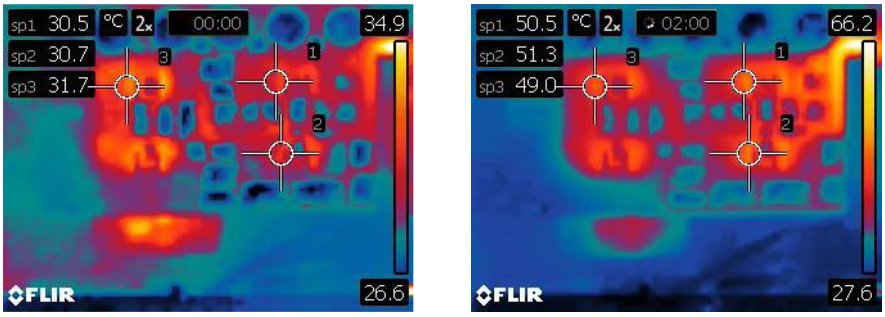
Fig. 5.10: Working waveforms of the DAB converter with (a) conventional EPS modulation (b) modified EPS modulation, both with $D_\varphi = 0.33$.



(a) (b)

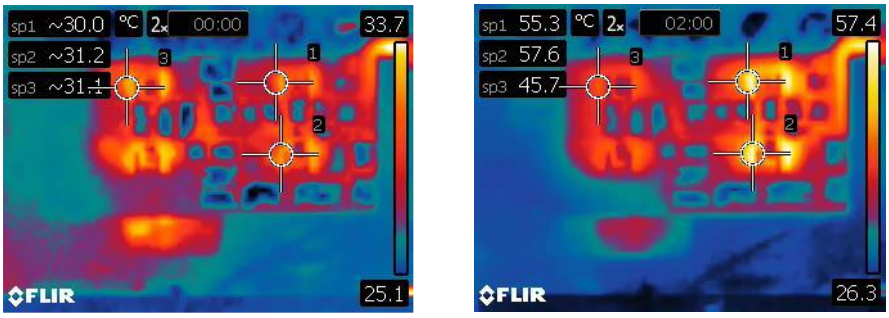
Fig. 5.11: Case temperatures measurement of Q_5, Q_6 and Q_8 at (a) initial state (b) final state without thermal control for $P_o = 320\ W$, $D_\varphi = 0.19$.

the measured case temperatures are shown in Fig. 5.11 and Fig. 5.12, where the active thermal control is deactivated and activated, respectively. It can be seen that the most



(a) (b)

Fig. 5.12: Case temperature measurements of Q_5, Q_6 and Q_8 at (a) initial state (b) final state with thermal control for $P_o = 320\ W$, $D_\varphi = 0.19$.



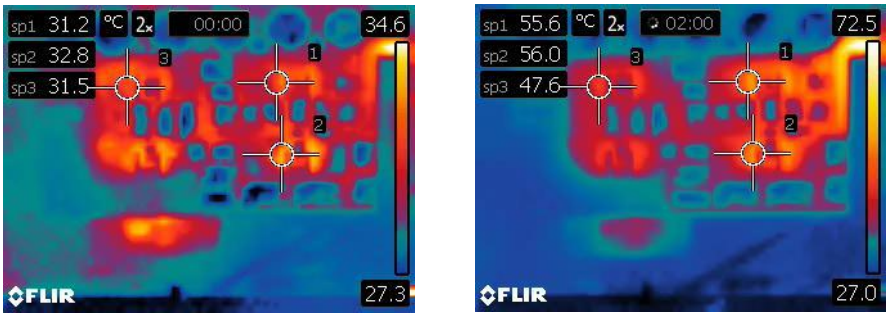
(a) (b)

Fig. 5.13: Case temperature measurements of Q_5, Q_6 and Q_8 at (a) initial state (b) final state without thermal control for $P_o = 360\ W$, $D_\varphi = 0.25$.

stressed power device in conventional EPS modulation is Q_8 with a case temperature of 52.5^oC (cf. sp2 in Fig. 5.11(b) and Q_8 in Fig. 5.8(b)). After applying the active thermal control, the final case temperature of Q_8 is reduced to 51.3^oC, as shown in Fig. 5.12(b).

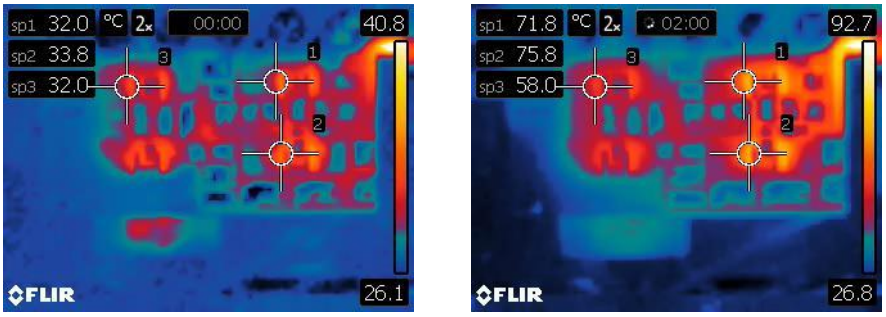
In the second group, the output power is increased to 360 W, and the experimental results are shown in Fig. 5.13 and Fig. 5.14. Q_8 is still the most stressed power device and the case temperature $T_{c,Q8}$ is reduced from 57.5^oC (cf. Fig. 5.13(b)) to 56.0^oC (cf. Fig. 5.14(b)). Note that the initial $T_{j,Q8}$ in the conventional EPS modulation is lower than that in the hybrid EPS modulation, which are 31.2^oC (cf. Fig. 5.13(a)) and 32.8^oC (cf. Fig. 5.14(a)), respectively. By comparing the temperature difference between the initial state and the final state of Q_8, the effect of the active thermal control becomes stronger rather than only comparing the final state temperatures.

In the third group, a higher output power of 420 W is applied, and case temperature of Q_8 is reduced from 75.8^oC (cf. Fig. 5.15(b)) to 72.0^oC (cf. Fig. 5.16(b)) by using active thermal control. Meanwhile, the case temperature of Q_5 (cf. Fig. 5.8(b) and sp3



(a) (b)

Fig. 5.14: Case temperature measurements of Q_5, Q_6 and Q_8 at (a) initial state (b) final state with thermal control for $P_o = 360\ W$, $D_\varphi = 0.25$.

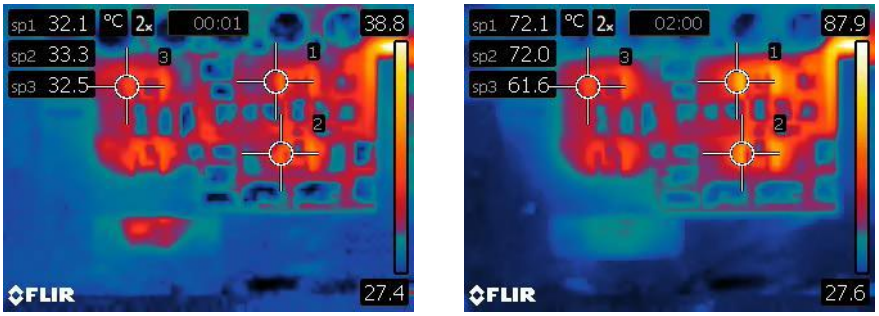


(a) (b)

Fig. 5.15: Case temperature measurements of Q_5, Q_6 and Q_8 at (a) initial state (b) final state without thermal control for $P_o = 420\ W$, $D_\varphi = 0.33$.

in Fig. 5.15(b)) in the final states are increased due to the longer conduction time in one switching period, as shown by the 56.0^oC in Fig. 5.15(b) and the 61.6^oC in Fig. 5.16(b).

For a clear overview of the case temperatures at initial and final states, the experimental results in Fig. 5.11 $\sim$ Fig. 5.16 are summarized in Table 5.3. The temperature increments between the initial and final case temperatures are also calculated and listed in Table. 5.3. It can be seen that the most stressed Q_8 has a larger temperature increment $\Delta T_{c,Q8}$ with higher output power, and the effect of active thermal control becomes more clear by comparing the values of $\Delta T_{c,Q8}$ in each group. Compared to the conventional (Conv.) EPS modulation, the temperature increment $\Delta T_{c,Q8}$ is lowered by utilizing the hybrid (Hybr.) EPS modulation, where the active thermal control is activated. In detail, a difference of 1.3^oC, 3.2^oC and 3.3^oC can be observed between the Conv. and Hybr. experiments for the three output powers of 320 W, 360 W and 420 W, respectively.



(a) (b)

Fig. 5.16: Case temperature measurements of Q_5, Q_6 and Q_8 at (a) initial state (b) final state with thermal control for $P_o = 420\ W$, $D_\varphi = 0.33$.

Table 5.3: Summary of the Measured Initial and Final Case Temperatures of Q_5, Q_6 and Q_8 with Different Control Methods and Output Power Levels

		$T_{c,Q6}$	$\boldsymbol{T_{c,Q8}}$	$T_{c,Q5}$	$\Delta T_{c,Q6}$	$\boldsymbol{\Delta T_{c,Q8}}$	$\Delta T_{c,Q5}$
Conv. 320 W	Initial	30.3^oC	$\mathbf{30.7^oC}$	31.7^oC	21.0^oC	$\mathbf{21.9^oC}$	18.3^oC
$\rightarrow$ Fig. 5.11	Final	51.3^oC	$\mathbf{52.6^oC}$	50.0^oC			
Hybr. 320 W	Initial	30.5^oC	$\mathbf{30.7^oC}$	31.7^oC	20.0^oC	$\mathbf{20.6^oC}$	17.3^oC
$\rightarrow$ Fig. 5.12	Final	50.5^oC	$\mathbf{51.3^oC}$	49.0^oC			
Conv. 360 W	Initial	30.0^oC	$\mathbf{31.2^oC}$	31.1^oC	25.3^oC	$\mathbf{26.4^oC}$	14.6^oC
$\rightarrow$ Fig. 5.13	Final	55.3^oC	$\mathbf{57.6^oC}$	45.7^oC			
Hybr. 360 W	Initial	31.2^oC	$\mathbf{32.8^oC}$	31.5^oC	24.4^oC	$\mathbf{23.2^oC}$	16.1^oC
$\rightarrow$ Fig. 5.14	Final	55.6^oC	$\mathbf{56.0^oC}$	47.6^oC			
Conv. 420 W	Initial	32.0^oC	$\mathbf{33.8^oC}$	32.0^oC	39.8^oC	$\mathbf{42.0^oC}$	26.0^oC
$\rightarrow$ Fig. 5.15	Final	71.8^oC	$\mathbf{75.8^oC}$	58.0^oC			
Hybr. 420 W	Initial	32.1^oC	$\mathbf{33.3^oC}$	32.5^oC	40.0^oC	$\mathbf{38.7^oC}$	29.1^oC
$\rightarrow$ Fig. 5.16	Final	72.1^oC	$\mathbf{72.0^oC}$	61.6^oC			

5.5 Summary

A hybrid extended-phase-shift modulation method is introduced to actively control the thermal stresses of the power devices. In this method, the conventional EPS modulation or the modified EPS modulation is adopted according to temperature of the most stressed power device. By re-configuring the conduction time of each power device in one switching period, a good thermal balance can be achieved without sac-

rificing other converter performances such as efficiency. The theoretical analysis is validated using the simulation and experimental results.

Chapter 6

Conclusions

6.1 Summary

Focusing on the DC-DC conversion stage in the on-board charger application, the Ph.D project selects the dual-active-bridge (DAB) converter as the research target. Different aspects concerning the DAB converter is studied in order to make it more applicable to practical situations. In such way this research is expected to facilitate the advancement of the OBC for future EV. A brief summary of this Ph.D thesis is as follows.

In Chapter 1, the research background is firstly introduced starting from the increasing sales of EV worldwide to the charging techniques for EV. A brief top-down introduction about the off-/on-board charger (OBC), integrated-/standalone-OBC and single-/two-stage standalone OBC is presented. Then a few popular bidirectional isolated DC-DC converters are compared, leading to the final selection of the DAB converter as the research target because of lower component numbers, symmetrical circuit structure and the capability of higher power density. Next, the research questions and relevant research objectives are aroused corresponding to the challenges for OBC application.

In Chapter 2, an improved DAB model is presented using the generalized average modeling (GAM) technique. Various power loss sources are incorporated in this model and thus an accurate mapping relationship from the controlled phase shift to the output dc voltage is achieved. In addition, a universal generalized average model considering arbitrary harmonic components is derived and on this basis, the effect of the 3^{rd}-order harmonic component of the leakage inductance current on the modeling accuracy is highlighted in light-loading situations. This effect and the modeling accuracy are addressed by experimental results.

In Chapter 3, an accurate calculation method is developed to define the ZVS boundary under varying dc voltages and charging powers. Based on the practical switching transients, the ZVS transition principle is analyzed firstly taking into account the non-linearity of the output capacitance of the power device. Due to the simultaneous turning-on/turning-off of the two power devices in the same leg, the

respective discharging/charging procedures is analyzed at the same time. Then the exchange of the charges between the output capacitance and the leakage inductance current is precisely calculated in order to identify the minimum peak current at the switching instants. Together with the operating mode of the DAB converter, which is determined by the power transfer requirement, the ZVS limitation on the control variables are attained. Finally, a comprehensive validation is implemented with numerous experimental cases.

In order to achieve the both targets of reduced conduction losses and simplified control procedure, Chapter 4 discusses a linear control strategy using a hybrid modulation. The losses distribution of the built DAB prototype is firstly calculated, and the results show that the conduction losses dominate the total power losses owing to the soft-switching realization. Then the complex relationship among the controlled multiple phase shifts is deduced to achieve the minimum conduction losses, which will further complicate the closed-loop real-time control. Aiming to decrease the computational burden, the relationship is linearized by combining the extended phase-shift and single-phase-shift modulation schemes. The optimization scheme is then validated by operating the DAB converter with different power levels.

In Chapter 5, an active thermal control method is proposed for the purpose of reducing the thermal loading of the most stressed power devices in the converter. By utilizing the redundant modulation vector, a modified modulation scheme is employed to regulate the conduction losses. Hence the power losses are redistributed among the power devices. The active thermal management is applied to the converter and by comparing the measured case temperatures with the conventional and the proposed modulation schemes in experiments, it proves the correctness of the theoretical analysis.

6.2 Main Contributions

Following th research questions and tasks in Chapter 1, the main contributions of this PhD project can be summarized as follows:

A. Accurate generalized average modeling of the DAB converter

- Compared to the prior-art DAB lossless models or only partial losses are included, a practical DAB model considering various power losses including the conduction loss, core loss and capacitor loss is built.
- A universal generalized average model that incorporates any harmonic components are also derived.
- Instead of the commonly used first harmonic approximation (FHA) in previous literature, the 3^{rd}-order harmonic is found to be more prominent in light loading situations.

B. Accurate calculation of the ZVS boundary

- Rather than analyzing only one power device, which is about to softly turn on at the switching transition, an analysis method considering both power devices on the same leg is proposed. On this basis, the concepts of

equivalent output capacitance and equivalent charge are introduced for analysis.

- In the current methods of ZVS calculation, the non-linear output capacitance of the power device is either neglected or improperly considered. As an enhanced calculation method, the non-linear variation of the output capacitance is precisely described during the measured switching transients.
- A comprehensive comparison among the prior-art and the proposed methods is implemented and validated by numerous experimental cases using different system parameters.

C. Simplified control scheme to reduce the conduction losses

- All possible operating modes with the extended-phase-shift modulation scheme are summarized under the voltage boost and buck situations.
- The power transfer range and conventional ZVS limitations for all possible operation modes are analytically expressed.
- A linear hybrid modulation scheme is proposed to simply the complex control procedure and meanwhile achieve the optimization objective of the losses reduction.

D. Active thermal control for an improved converter reliability

- The effects of the conventional modulation scheme on the thermal loading of the power device are analyzed and illustrated by unbalanced case temperatures in experiments.
- Instead of using a fixed 50% duty cycle of the driving signals as explained in the literature, a modified modulation scheme with different duty cycles for driving the power devices is proposed without sacrificing other converter performances.
- The case temperature of the most stressed power device is effectively reduced in the experimental validation.

6.3 Research Perspectives and Future Work

This Ph.D project investigated different aspects of the DAB converter for OBC application, and relevant methods for a better converter performance are proposed. However, there are still some other challenges that are worth to research, as listed in the following.

- A large-signal continuous-time model is built in this project. However, regarding the controller design and the stability analysis of the DAB converter, a discrete small-signal model is necessary to investigate the effect of controller parameters on the dynamics response of the converter. Besides, the switching frequency is increasing with the application of wide-band-gap (WBG) power devices. On this basis, the proportions of the sampling time and dead time over the switching period become larger, this may challenge the converter control and is worth to study more .

- There are various on-board charging power levels such as 3.3 kW, 6.6 kW and 22 kW. The electric vehicle can be charged with different powers depending on the available charging infrastructure. For example, the Toyota Prius integrates the three charging power levels mentioned above into one on-board charger. However, most power electronic converters are designed for achieving the highest efficiency at the rated power, and the efficiency will decrease with lower or heavier power load. Therefore, a proper design of the OBC to achieve a flat and high efficiency curve over a wide charging power range is worth to study. Actually, one way to achieve this is to utilize the concept of modular design. By sharing the required power among several DAB modules rather than in one single converter, the power losses can be considerably decreased and thus the goal of a flat efficiency curve can be realized.
- This Ph.D project focuses on the DC-DC conversion of the OBC and selects the DAB converter as the research target. However, the AC-DC conversion from single-phase or three-phase AC grid input to the DC-link output is also an important part of the OBC, which is closely related to the grid-connection power quality and energy exchange between the battery and the grid. Especially, if the rectifier can also achieve soft-switching, the whole OBC efficiency will be further increased. Moreover, considering the limited space in an EV, a compact design of OBC is often required and the OBC can become more adaptive if it can allow various charging powers. One practical method to achieve this is to integrate single-phase and three-phase charging in the same circuit. On this basis, relevant circuit design and control methods are expected to be developed.
- In this Ph.D project, the proposed active thermal control can reduce the thermal loading of the most stressed power device. This can improve the converter reliability considering the high ambient temperature under the hood in an EV. However, another more important factor related to the power semiconductor reliability is the thermal cycling for a specific mission profile. This results in the junction temperature swing, which can further lead to device failures such as solder cracking and bond wire liftoff. Therefore, the method that can reduce the temperature swing is worth to research more.
- This Ph.D project only researches the component-level reliability improvement, specially the power semiconductor. In the design of an OBC, the manufacturers cares more about the system-level reliability under required operating conditions, i.e. mission profile. For example, uncertain charging profiles caused by available charging connectors and consumer habits can generate different lifetime prediction results for the same OBC. Besides, the uncertainty of the OBC can also be caused by the parameter variation of the power semiconductors, passive components (e.g. capacitors and transformers), battery pack and other circuit components. Therefore, a mission-profile-based reliability assessment of the whole OBC is absent and worth to study more for the further popularization of EVs around the world.

Chapter 7

Bibliography

References

[1] "Global ev outlook 2020," International Energy Agency, Paris, Tech. Rep., 2020, available: https://www.iea.org/reports/global-ev-outlook-2020.

[2] G. R. Chandra Mouli, J. Schijffelen, M. van den Heuvel, M. Kardolus, and P. Bauer, "A 10 kW solar-powered bidirectional EV charger compatible with chademo and combo," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1082–1098, 2019.

[3] C. Hamilton, G. Gamboa, J. Elmes, R. Kerley, A. Arias, M. Pepper, J. Shen, and I. Batarseh, "System architecture of a modular direct-dc pv charging station for plug-in electric vehicles," in *IECON 2010-36th Annual Conference on IEEE Industrial Electronics Society*. IEEE, 2010, pp. 2516–2520.

[4] G. Carli and S. S. Williamson, "Technical considerations on power conversion for electric and plug-in hybrid electric vehicle battery charging in photovoltaic installations," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5784–5792, 2013.

[5] G. R. C. Mouli, M. Leendertse, V. Prasanth, P. Bauer, S. Silvester, S. van de Geer, and M. Zeman, "Economic and co2 emission benefits of a solar powered electric vehicle charging station for workplaces in the netherlands," in *2016 IEEE Transportation Electrification Conference and Expo (ITEC)*. IEEE, 2016, pp. 1–7.

[6] B. V. Bakolas, P. Bauer, and D. Prins, "Testing of smart charging controller for dynamic charging from solar panels," in *2014 IEEE Transportation Electrification Conference and Expo (ITEC)*. IEEE, 2014, pp. 1–4.

[7] D. Van der Meer, G. R. C. Mouli, G. M.-E. Mouli, L. R. Elizondo, and P. Bauer, "Energy management system with pv power forecast to optimally charge evs at the workplace," *IEEE Trans. Ind. Informat.*, vol. 14, no. 1, pp. 311–320, 2016.

[8] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, 2012.

[9] J. Nisewanger, "Viral article on tesla bidirectional ac charging is "debunked"," Electric Revs, Tech. Rep., 2020. [Online] Available: https://electricrevs.com/2020/05/21/viral-article-on-tesla-bidirectional-ac-charging-is-debunked/.

[10] A. G. Cocconi, "Combined motor drive and battery recharge system," ed: Google Patents Patent, 1994.

[11] S. Haghbin, S. Lundmark, M. Alakula, and O. Carlson, "Grid-connected integrated battery chargers in vehicle applications: Review and new solution," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 459–473, 2012.

[12] A. P. Sandulescu, F. Meinguet, X. Kestelyn, E. Semail, and A. Bruyere, "Flux-weakening operation of open-end winding drive integrating a cost-effective high-power charger," *IET Electr Syst Transp*, vol. 3, no. 1, pp. 10–21, 2013.

[13] I. Subotic, N. Bodo, E. Levi, B. Dumnic, D. Milicevic, and V. Katic, "Overview of fast on-board integrated battery chargers for electric vehicles based on multiphase machines and power electronics," *IET Electr Power Appl*, vol. 10, no. 3, pp. 217–229, 2016.

[14] R. Shi, S. Semsar, and P. W. Lehn, "Constant current fast charging of electric vehicles via a DC grid using a dual-inverter drive," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 6940–6949, 2017.

[15] G. Su, C. White, and Z. Liang, "Design and evaluation of a 6.6 kW GaN converter for onboard charger applications," in *Proc. IEEE 18th Workshop Control and Modeling for Power Electronics (COMPEL)*, 2017, pp. 1–6.

[16] E. Levi, R. Bojoi, F. Profumo, H. A. Toliyat, and S. Williamson, "Multiphase induction motor drives - a technology status review," *IET Electr Power Appl*, vol. 1, no. 4, pp. 489–516, 2007.

[17] S. Y. Kim, H. Song, and K. Nam, "Idling port isolation control of three-port bidirectional converter for evs," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2495–2506, 2012.

[18] S. Sae, "Electric vehicle and plug in hybrid electric vehicle conductive charge coupler," 2010.

[19] B. Li, Q. Li, F. C. Lee, Z. Liu, and Y. Yang, "A high-efficiency high-density wide-bandgap device-based bidirectional on-board charger," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1627–1636, 2018.

[20] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM converter power density barriers," in *Proc. Power Conversion Conf. - Nagoya*, 2007, pp. P–9–P–29.

[21] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal ZVS modulation of single-phase single-stage bidirectional DAB AC–dc converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3954–3970, Aug. 2014.

[22] and Byeongwoo Kim, Minjae Kim, and S. Choi, "Single-stage electrolytic capacitor-less AC-DC converter with high frequency isolation for EV charger," in *Proc. IEEE 8th Int. Power Electronics and Motion Control Conf. (IPEMC-ECCE Asia)*, 2016, pp. 234–238.

[23] N. D. Weise, G. Castelino, K. Basu, and N. Mohan, "A single-stage dual-active-bridge-based soft switched AC–dc converter with open-loop power factor correction and other advanced features," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4007–4016, 2014.

[24] J. Lu, Q. Tian, K. Bai, A. Brown, and M. McAmmond, "An indirect matrix converter based 97%-efficiency on-board level 2 battery charger using e-mode GaN hemts," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 351–358.

[25] J. Lu, K. Bai, A. R. Taylor, G. Liu, A. Brown, P. M. Johnson, and M. McAmmond, "A modular-designed three-phase high-efficiency high-power-density EV battery charger using dual/triple-phase-shift control," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8091–8100, 2018.

[26] F. Jauch and J. Biela, "Combined phase-shift and frequency modulation of a dual-active-bridge AC–dc converter with pfc," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8387–8397, 2016.

[27] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless pfc boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, 2008.

[28] Q. Huang and A. Q. Huang, "Review of gan totem-pole bridgeless pfc," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 187–196, 2017.

[29] Z. Ye, A. Agular, Y. Bolurian, and B. Daugherty, "Gan fet-based ccm totem-pole bridgeless pfc," in *Texas Instruments Power Supply Design Seminar*, 2014.

[30] W. Kempton and J. Tomić, "Vehicle-to-grid power implementation: From stabilizing the grid to supporting large-scale renewable energy," *J Power Sources*, vol. 144, no. 1, pp. 280–294, 2005.

[31] J. R. Pillai and B. Bak-Jensen, "Integration of vehicle-to-grid in the western danish power system," *IEEE Trans. Sustain. Energy*, vol. 2, no. 1, pp. 12–19, 2010.

[32] M. C. Kisacikoglu, B. Ozpineci, and L. M. Tolbert, "Examination of a phev bidirectional charger system for v2g reactive power compensation," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2010, pp. 458–465.

[33] H. Lund and W. Kempton, "Integration of renewable energy into the transport and electricity sectors through v2g," *Energy policy*, vol. 36, no. 9, pp. 3578–3587, 2008.

[34] G. R. C. Mouli, J. Kaptein, P. Bauer, and M. Zeman, "Implementation of dynamic charging and v2g using chademo and ccs/combo dc charging standard," in *2016 IEEE Transportation Electrification Conference and Expo (ITEC)*. IEEE, 2016, pp. 1–6.

[35] H. Xiao and S. Xie, "A zvs bidirectional dc–dc converter with phase-shift plus pwm control scheme," *IEEE Trans Power Electron*, vol. 23, no. 2, pp. 813–823, 2008.

[36] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 174–182, 1988.

[37] K. Karube, T. Nomura, and T. Nakano, "High frequency resonant MOS-FET DC-dc converter," in *Proc. th Annual IEEE Power Electronics Specialists Conf. PESC '88 Record*, 1988, pp. 26–32 vol.1.

[38] R. P. Severns, "Topologies for three-element resonant converters," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 89–98, 1992.

[39] S. Haghbin, M. Alatalo, F. Yazdani, T. Thiringer, and R. Karlsson, "The design and construction of transformers for a 50 kw three-phase dual active bridge dc/dc converter." IEEE, 2017, pp. 1–5.

[40] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high power density DC/dc converter for high power applications," in *Proc. Conf. Record of the 1988 IEEE Industry Applications Society Annual Meeting*, 1988, pp. 796–805 vol.1.

[41] F. Krismer, "Modeling and optimization of bidirectional dual active bridge dc-dc converter topologies," Ph.D. dissertation, ETH Zürich, Zürich, Switzerland, 2010.

[42] N. Schibli, "Symmetrical multilevel converters with two quadrant dc-dc feeding," EPFL, Tech. Rep., 2000.

[43] M. S. Islam and N. Mithulananthan, "Daily ev load profile of an ev charging station at business premises," in *2016 IEEE Innovative Smart Grid Technologies-Asia (ISGT-Asia)*. IEEE, 2016, pp. 787–792.

[44] J. Meng, L. Cai, D.-I. Stroe, G. Luo, X. Sui, and R. Teodorescu, "Lithium-ion battery state-of-health estimation in electric vehicle using optimized partial charging voltage profiles," *Energy*, vol. 185, pp. 1054–1062, 2019.

[45] Y. Wang, X. Dai, G. Liu, Y. Wu, Y. Li, and S. Jones, "Status and trend of power semiconductor module packaging for electric vehicles," *Modeling and Simulation for Electric Vehicle Applications*, p. 23, 2016.

[46] A. Goswami, "Thermal management of on-board chargers in e-vehicles," Tech. Rep., 2017. [Online]. Available: https://www.electronics-cooling.com/2017/08/thermal-management-board-chargers-e-vehicles/

[47] S. S. Ang and H. A. Mantooth, *Reliability of Power Electronic Converter Systems*. The Institution of Engineering and technology, London, United Kingdom, 2015, ch. Reliability of power electronic packaging, pp. 94–97.

[48] C. Zhao, S. D. Round, and J. W. Kolar, "Full-order averaging modelling of zero-voltage-switching phase-shift bidirectional DC-dc converters," *IET Power Electron*, vol. 3, no. 3, pp. 400–410, May 2010.

[49] F. Krismer and J. W. Kolar, "Accurate small-signal model for an automotive bidirectional dual active bridge converter," in *Proc. 11th Workshop Control and Modeling for Power Electronics*, Aug. 2008, pp. 1–10.

[50] L. Shi, W. Lei, Z. Li, J. Huang, Y. Cui, and Y. Wang, "Bilinear discrete-time modeling and stability analysis of the digitally controlled dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8787–8799, Nov. 2017.

[51] D. Costinett, "Reduced order discrete time modeling of ZVS transition dynamics in the dual active bridge converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, Mar. 2015, pp. 365–370.

[52] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *Proc. IEEE Power Electronics Specialists Conference*, Jun. 1976, pp. 18–34.

[53] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 251–259, Apr. 1991.

[54] J. A. Mueller and J. W. Kimball, "An improved generalized average model of dc–dc dual active bridge converters," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9975–9988, Nov. 2018.

[55] H. Qin and J. W. Kimball, "Generalized average modeling of dual active bridge DC–dc converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2078–2084, Apr. 2012.

[56] K. Zhang, Z. Shan, and J. Jatskevich, "Large-and small-signal average-value modeling of dual-active-bridge dc–dc converter considering power losses," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1964–1974, Mar. 2016.

[57] H. Bai, C. Mi, C. Wang, and S. Gargies, "The dynamic model and hybrid phase-shift control of a dual-active-bridge converter," in *Proc. 34th Annual Conf. of IEEE Industrial Electronics*, Nov. 2008, pp. 2840–2845.

[58] F. Krismer and J. W. Kolar, "Accurate small-signal model for the digital control of an automotive bidirectional dual active bridge," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2756–2768, Dec. 2009.

[59] V. A. Caliskan, O. C. Verghese, and A. M. Stankovic, "Multifrequency averaging of DC/dc converters," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 124–133, Jan. 1999.

[60] H. Chung, S. Y. R. Hui, and K. K. Tse, "Reduction of power converter EMI emission using soft-switching technique," *IEEE Trans. Electromagn. Compat.*, vol. 40, no. 3, pp. 282–287, Aug. 1998.

[61] R. Li, Q. Zhu, and M. Xie, "A new analytical model for predicting dv/dt-induced low-side MOSFET false turn-on in synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5500–5512, Jun. 2019.

[62] G. Oggier, G. O. García, and A. R. Oliva, "Modulation strategy to operate the dual active bridge DC-dc converter under soft switching in the whole operating range," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1228–1236, Apr. 2011.

[63] S. S. Shah, V. M. Iyer, and S. Bhattacharya, "Exact solution of ZVS boundaries and AC-port currents in dual active bridge type DC–dc converters," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5043–5047, Jun. 2019.

[64] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando, and J. Sebastián, "Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 790–804, Feb. 2015.

[65] J. Everts, "Closed-form solution for efficient ZVS modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7561–7576, Oct. 2017.

[66] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[67] *Power MOSFET Electrical Characteristics*, TOSHIBA, Jul. 2018.

[68] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.

[69] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. Rivas-Davila, "Coss losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10 748–10 763, Dec. 2018.

[70] M. Guacci, M. Heller, D. Neumayr, D. Bortis, J. W. Kolar, G. Deboy, C. Ostermaier, and O. Häberlen, "On the origin of the c_{oss} -losses in soft-switching GaN-on-si power hemts," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 679–694, Jun. 2019.

[71] Z. Chen, D. Boroyevich, R. Burgos, and F. Wang, "Characterization and modeling of 1.2 kv, 20 A SiC mosfets," in *Proc. IEEE Energy Conversion Congress and Exposition*, Sep. 2009, pp. 1480–1487.

[72] Z. Shen, R. Burgos, D. Boroyevich, and F. Wang, "Soft-switching capability analysis of a dual active bridge dc-dc converter," in *Proc. IEEE Electric Ship Technologies Symp*, Apr. 2009, pp. 334–339.

[73] R. D. Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high power density DC/DC converter for high power applications," in *Conference Record of the 1988 IEEE Industry Applications Society Annual Meeting*. IEEE, 1988.

[74] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC–DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, Mar. 2012.

[75] S. Inoue and H. Akagi, "A bidirectional DC–DC converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, Nov. 2007.

[76] X. Wang, F. Tian, and I. Batarseh, "High efficiency parallel post regulator for wide range input DC–dc converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 852–858, Mar. 2008.

[77] J. Biela, U. Badstuebner, and J. W. Kolar, "Impact of power density maximization on efficiency of DC–dc converter systems," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 288–300, Jan. 2009.

[78] N. M. L. Tan, N. M. L. Tan, S. Inoue, S. Inoue, A. Kobayashi, and H. Akagi, "Voltage balancing of a 320-V, 12-F electric double-layer capacitor bank combined with a 10-kW bidirectional isolated DC–DC converter," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2755–2765, Nov. 2008.

[79] M. B. Camara, H. Gualous, F. Gustin, A. Berthon, and B. Dakyo, "DC/dc converter design for supercapacitor and battery power management in hybrid vehicle applications—polynomial control strategy," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 587–597, Feb. 2010.

[80] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift control of isolated bidirectional DC–dc converter for power distribution in microgrid," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4667–4680, Nov. 2012.

[81] F. Li, Y. Li, and X. You, "Optimal dual-phase-shift control strategy of an isolated buck–boost converter with a clamped inductor," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5374–5385, Jun. 2018.

[82] B. Liu, P. Davari, and F. Blaabjerg, "A flexible control scheme for single-stage DAB AC/DC converters," in *Proc. IEEE Int. Power Electronics and Application Conf. and Exposition (PEAC)*, Nov. 2018, pp. 1–6.

[83] X. Liu, Z. Q. Zhu, D. A. Stone, M. P. Foster, W. Q. Chu, I. Urquhart, and J. Greenough, "Novel dual-phase-shift control with bidirectional inner phase shifts for a dual-active-bridge converter having low surge current and stable power control," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 4095–4106, May 2017.

[84] G. Xu, D. Sha, J. Zhang, and X. Liao, "Unified boundary trapezoidal modulation control utilizing fixed duty cycle compensation and magnetizing current design for dual active bridge DC–dc converter," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2243–2252, Mar. 2017.

[85] B. Liu, P. Davari, and F. Blaabjerg, "An optimized control scheme to reduce the backflow power and peak current in dual active bridge converters," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2019, pp. 1622–1628.

[86] C. Calderon, A. Barrado, A. Rodriguez, P. Alou, A. Lazaro, C. Fernandez, and P. Zumel, "General analysis of switching modes in a dual active bridge with triple phase shift modulation," *Energies*, vol. 11, no. 9, p. 2419, 2018.

[87] O. M. Hebala, A. A. Aboushady, K. H. Ahmed, and I. Abdelsalam, "Generic closed-loop controller for power regulation in dual active bridge DC–dc converter with current stress minimization," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4468–4478, Jun. 2019.

[88] B. Zhao, Q. Song, W. Liu, and W. Sun, "Current-stress-optimized switching strategy of isolated bidirectional DC–dc converter with dual-phase-shift control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4458–4467, Oct. 2013.

[89] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified triple-phase-shift control to minimize current stress and achieve full soft-switching of isolated bidirectional DC–dc converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.

[90] N. Hou, W. Song, and M. Wu, "Minimum-current-stress scheme of dual active bridge DC–dc converter with unified phase-shift control," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8552–8561, Dec. 2016.

[91] Q. Gu, L. Yuan, J. Nie, J. Sun, and Z. Zhao, "Current stress minimization of dual-active-bridge DC–dc converter within the whole operating range," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 129–142, Mar. 2019.

[92] H. Shi, H. Wen, J. Chen, Y. Hu, L. Jiang, G. Chen, and J. Ma, "Minimum-backflow-power scheme of DAB-based solid-state transformer with extended-phase-shift control," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3483–3496, Jul. 2018.

[93] H. Wen, W. Xiao, and B. Su, "Nonactive power loss minimization in a bidirectional isolated DC–dc converter for distributed power systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6822–6831, Dec. 2014.

[94] A. Tong, L. Hang, G. Li, X. Jiang, and S. Gao, "Modeling and analysis of a dual-active-bridge-isolated bidirectional DC/dc converter to minimize RMS current with whole operating range," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5302–5316, Jun. 2018.

[95] S. Chakraborty and S. Chattopadhyay, "Minimum-RMS-current operation of asymmetric dual active half-bridge converters with and without ZVS," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5132–5145, Jul. 2017.

[96] W. Choi, K. Rho, and B. Cho, "Fundamental duty modulation of dual-active-bridge converter for wide-range operation," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4048–4064, Jun. 2016.

[97] G. G. Oggier and M. Ordonez, "High-efficiency DAB converter using switching sequences and burst mode," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2069–2082, Mar. 2016.

[98] J. Hiltunen, V. Väisänen, R. Juntunen, and P. Silventoinen, "Variable-frequency phase shift modulation of a dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7138–7148, Dec. 2015.

[99] W. A. Roshen, "A practical, accurate and very general core loss model for non-sinusoidal waveforms," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 30–40, Jan. 2007.

[100] M. P. D. Graovac and A. Kiep, "Mosfet power losses calculation using the datasheet parameters," Available online at https://www.infineon.com, Tech. Rep., 2008.

[101] F. Blaabjerg, Zhe Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, 2004.

[102] M. Liserre, T. Sauter, and J. Y. Hung, "Future energy systems: Integrating renewable energy sources into the smart power grid through industrial electronics," *IEEE Ind. Electron. Mag.*, vol. 4, no. 1, pp. 18–37, 2010.

[103] A. Emadi, Y. J. Lee, and K. Rajashekara, "Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237–2245, 2008.

[104] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97–114, 2014.

[105] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, 2011.

[106] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, 2010.

[107] M. Andresen, M. Schloh, G. Buticchi, and M. Liserre, "Computational light junction temperature estimator for active thermal control," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7.

[108] A. Matallana, E. Ibarra, I. López, J. Andreu, J. Garate, X. Jorda, and J. Rebollo, "Power module electronics in hev/ev applications: New trends in wide-bandgap semiconductor technologies and design aspects," *Renewable Sustainable Energy Rev*, vol. 113, p. 109264, 2019.

[109] P. Jacob, "Early life field failures in modern automotive electronics–an overview; root causes and precautions," *Microelectron Reliab*, vol. 64, pp. 79–83, 2016.

[110] F. H. Gandoman, A. Ahmadi, P. Van den Bossche, J. Van Mierlo, N. Omar, A. E. Nezhad, H. Mavalizadeh, and C. Mayet, "Status and future perspectives of reliability assessment for electric vehicles," *Reliability Engineering & System Safety*, vol. 183, pp. 1–16, 2019.

[111] Y. Yang, H. Wang, A. Sangwongwanich, and F. Blaabjerg, "Design for reliability of power electronic systems," in *Power electronics handbook*. Elsevier, 2018, pp. 1423–1440.

[112] F. Blaabjerg, D. Zhou, A. Sangwongwanich, and H. Wang, "Design for reliability in renewable energy systems," in *2017 International Symposium on Power Electronics (Ee)*. IEEE, 2017, pp. 1–6.

[113] Y. Ko, M. Andresen, G. Buticchi, and M. Liserre, "Discontinuous-modulation-based active thermal control of power electronic modules in wind farms," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 301–310, 2018.

[114] A. Isidori, F. M. Rossi, F. Blaabjerg, and K. Ma, "Thermal loading and reliability of 10-MW multilevel wind power converter at different wind roughness classes," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 484–494, 2014.

[115] J. Sheng, H. Yang, C. Li, M. Chen, W. Li, X. He, and X. Gu, "Active thermal control for hybrid modular multilevel converter under overmodulation operation," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4242–4255, 2020.

[116] Z. Qin, P. C. Loh, and F. Blaabjerg, "Application criteria for nine-switch power conversion systems with improved thermal performance," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4608–4620, 2015.

[117] M. Andresen, M. Liserre, and G. Buticchi, "Review of active thermal and lifetime control techniques for power electronic modules," in *Proc. 16th European Conf. Power Electronics and Applications*, 2014, pp. 1–10.

[118] Z. Chen, J. M. Guerrero, and F. Blaabjerg, "A review of the state of the art of power electronics for wind turbines," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1859–1875, 2009.

[119] V. Raveendran, M. Andresen, and M. Liserre, "Improving onboard converter reliability for more electric aircraft with lifetime-based control," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5787–5796, 2019.

[120] and Zian Qin, M. Liserre, F. Blaabjerg, and Huai Wang, "Energy storage system by means of improved thermal performance of a 3 MW grid side wind power converter," in *Proc. IECON 2013 - 39th Annual Conf. of the IEEE Industrial Electronics Society*, 2013, pp. 736–742.

[121] M. Chen, H. Wang, D. Pan, X. Wang, and F. Blaabjerg, "Thermal characterization of silicon carbide MOSFET module suitable for high-temperature computationally-efficient thermal-profile prediction," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, p. 1, 2020.

[122] J. Falck, M. Andresen, and M. Liserre, "Active thermal control of IGBT power electronic converters," in *Proc. IECON 2015 - 41st Annual Conf. of the IEEE Industrial Electronics Society*, 2015, pp. 000 001–000 006.

[123] K. Ma, N. He, M. Liserre, and F. Blaabjerg, "Frequency-domain thermal modeling and characterization of power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7183–7193, 2016.

[124] H. Chen, B. Ji, V. Pickert, and W. Cao, "Real-time temperature estimation for power mosfets considering thermal aging effects," *IEEE Trans. Device Mater. Rel.*, vol. 14, no. 1, pp. 220–228, 2014.

[125] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Improved reliability of power modules: A review of online junction temperature measurement methods," *IEEE Ind. Electron. Mag.*, vol. 8, no. 3, pp. 17–27, 2014.

Selected Publications

Journal publication 1

An Optimized Hybrid Modulation Scheme for Reducing Conduction Losses in Dual Active Bridge Converters [J1]

B. Liu, P. Davari and F. Blaabjerg

The paper has been published in
IEEE Trans. Emerg. Sel. Topics Power Electron., Early Access, 2019.

The layout has been revised.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

An Optimized Hybrid Modulation Scheme for Reducing Conduction Losses in Dual Active Bridge Converters

Bochen Liu, *Student Member, IEEE,* Pooya Davari, *Senior Member, IEEE,* Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—A linearized hybrid modulation scheme for the DAB converter is proposed in this paper. For the purpose of minimizing the conduction losses dissipated on the transformer and the power transistors, an optimal relationship function between the two control variables employed in extended phase shift (EPS) modulation can be derived. However, the obtained relationship function is a complex expression, which is not good for simple online control. Hence, a linearized modulation scheme is proposed in this paper. This modulation scheme can achieve a quasi-minimum RMS value of the leakage inductance current for the same output power. Meanwhile, the zero voltage switching (ZVS) of the power transistors can be achieved over the whole power range. The power transfer capability is also kept same as the optimal EPS scheme. Finally, experiments are conducted on a laboratory prototype to validate the effect of the linearized modulation scheme on the reduction of conduction losses. The experimental results present an improved converter efficiency and the realization of ZVS.**

I. Introduction

Firstly proposed in 1988 [1], the dual active bridge (DAB) converter is now widely used in many applications such as distributed power systems and energy storage [2], [3]. Due to its advantages of galvanic isolation and bidirectional power flow, DAB converters are applied among multiple dc energy sources such as battery packs, ultra-capacitors and photovoltaic submodules to match various voltage levels [4]–[7]. Moreover, since the DAB converter can naturally achieve zero voltage switching (ZVS) without any auxiliary components and has a simple and symmetrical structure, it is also a potential candidate for high efficiency and high power density applications such as electric vehicles and aerospace [8]–[11]. For the same reason, the DAB is also an ideal dc-dc conversion choice for applications where modular design is often needed such as energy storage systems and power electronic transformers.

A conventional way to control the DAB converter is using single phase shift (SPS) modulation to fulfill the power/voltage/current requirements. SPS is simple and easy for real time control. However, utilizing this simple modulation scheme can not guarantee ZVS if the voltage ratio deviates far from one, which results in poor efficiency at partial load conditions. Notably, under this situation, even the switches might be broken with excessive dv/dt caused by ZVS failure [12]–[14]. In order to overcome this drawback, many improved modulation methods are introduced to extend the DAB soft-switching operating range, such as extended phase-shift (EPS) modulation [15], dual phase-shift (DPS) modulation [16], [17] and triple phase-shift (TPS) modulation [18]–[21]. Other than only one phase shift in SPS, these improved modulation schemes try to introduce more control variables.

In the simple SPS modulation, only the outer phase shift between the primary and the secondary full bridge is regulated, leading to a two-level primary and secondary winding voltage. If varying inner phase shift (as defined in Section II-B) is considered, the winding voltages turn to three-level because the diagonal switches in each full bridge are not turned on or off synchronously any more. Taking [21] as an example, a comprehensive searching of operation modes with TPS is implemented, and the corresponding soft-switching boundaries for each operation mode are derived. However, the analysis of power transfer range is absent, which is important for selecting proper operation mode due to the varying given powers.

Alternatively, applying multiple control variables makes it possible to realize a more ambitious target, such as current stress optimization [22]–[26], backflow power reduction [27] and non-active power loss minimization [28]. Actually, these optimization targets are based on optimizing different parts of the leakage inductance current, e.g. current stress optimization usually refers to reducing the peak value of the leakage inductance current, backflow power is often related to the intervals when the current direction is reversed into the power source.

Besides, many optimized control schemes are focusing on reducing the root mean square (RMS) value of the leakage inductance current [29]–[32], which is closely related to the conduction losses of the power semiconductors and high-frequency transformer. Notably, hybrid modulation methods could be adopted in order to extend the converter performance over a wide operation range [33], [34]. Furthermore, the switching frequency can also be varied aiming at specific optimization objects. In [35], the switching frequency is varied to modulate the DAB in a specific single-stage ac-dc converter. In [36], the circulating current is minimized over a wide power range using variable frequency modulation.

Among the aforementioned modulation methods, some of them are complicated and not easy to implement. One usual situation is that in order to make the DAB converter work at the optimal operation point, massive calculations are often conducted to handle those complex relationships among the

This paper is an extension of the conference paper with the title of "An Optimized Control Scheme for Reducing Conduction and Switching Losses in Dual Active Bridge Converters", which was presented in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), 2018.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

control variables. The reason is that at least three limitations should be taken into account during the operation, i.e. the ZVS range, the power transfer capability and the optimization targets. Of course, there exist other factors depending on different requirements, such as the voltage variation range, the transient response or the effect of the passive components. One way to solve the complexity is to adopt a look-up table in the control process, where the optimal operation points are calculated in advance and input into a table prior to the converter operation. But the performance of this method is adversely affected by the components mismatched parameters due to their tolerances, temperature dependency and lifetime. Moreover, a large memory is needed to guarantee the accuracy if the converter has to work in a wide operation range. In terms of the variable switching frequency modulation, one large challenge is the design of passive components and the electromagnetic interference filter.

In order to make the DAB converter more adaptive and applicable, this paper proposes an optimized hybrid modulation scheme to simplify the control process based on EPS modulation. The main contributions of this paper are:

- The comprehensive analysis of the power transfer range for each operation mode, which is derived based on the ZVS conditions rather than operation mode boundary conditions as in some literature.
- The analytical optimization expressions for each operation mode are derived in order to minimize the RMS value of the leakage inductance current.
- Several simplified optimization methods are proposed based on different voltage ratio requirements and preferred working conditions in various applications.
- Independent of the voltage ratio limitation and being simpler than other methods, the linearized optimization method is applied to the available DAB setup in this paper and validated by the experimental results.

This paper is organized as follows. Firstly, the EPS based operation modes for boost and buck scenarios under ZVS conditions are presented in Section II. Next, according to the derived operation modes in Section II and selected components for the DAB setup, the losses distribution are calculated in Section III. In Section IV, an optimal modulation scheme (called 'OMS1' in the following) is firstly derived. In order to simplify this scheme and considering different voltage ratio requirements, three approximated modulation schemes are developed. With the aim of selecting the most suitable modulation method, a through comparison is presented among these four schemes at the end of Section IV. Therefore, in Section V, the selected linear scheme is applied into a laboratory prototype to validate the feasibility on conduction losses reduction and ZVS realization. Finally, conclusions are given in Section VI.

II. Basic Modulation Methods for Dual Active Bridge Converters

A. DAB Model

The topology of the DAB converter is shown in Fig. 1. It consists mainly of two full bridges HB_1 and HB_2, the middle terminals of which are linked by a high-frequency transformer and the side ends are paralleled with the input and output dc voltage ports. In order to flexibly adjust the leakage inductance, an auxiliary inductor is cascaded with the high-voltage primary winding so that a lower additional power loss is induced compared to the secondary low-voltage high-current winding.

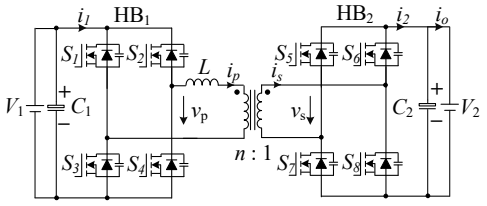


Fig. 1. Topology of the dual active bridge (DAB) converter.

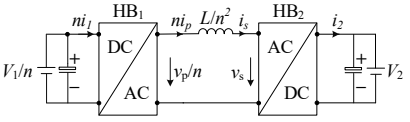


Fig. 2. Simplified DAB model by referring the converter to the secondary side of the transformer.

The magnetizing inductance is considered much larger than the leakage inductance, leading to negligible magnetizing current compared with the load current. Therefore in the T-type transformer equivalent circuit, the branch with magnetizing inductor can be seen as an open circuit. On this basis, the DAB model is obtained as shown in Fig. 2 after referring the circuit parameters to the secondary side.

B. Operation Modes

Due to the bidirectional power transfer ability and the symmetrical topology, the DAB converter has four operating scenarios: forward/backward, buck/boost. Assuming the power flow is from the primary side to the secondary side, a factor k is introduced as

$$k = \frac{V_1}{nV_2} \tag{1}$$

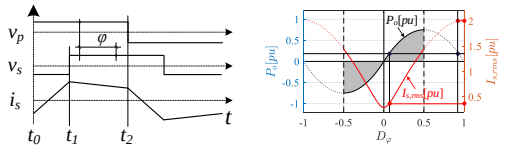
to signify the voltage ratio. $k < 1$ and $k > 1$ denote boost and buck scenarios, respectively.

In order to simplify the calculations, the base power P_b and base current I_b defined in (2) are used to normalize the real values. Therein, V_1, V_2 and f_{sw} denote the input, output dc voltage and the switching frequency, respectively. L is the total inductance consisting of the transformer leakage inductance and the auxiliary inductance.

$$P_b = \frac{(nV_2)^2}{8Lf_{sw}}, \quad I_b = \frac{n^2V_2}{8Lf_{sw}} \tag{2}$$

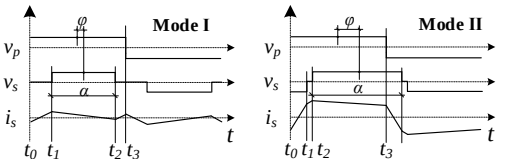
The power is mainly controlled by the outer phase shift φ, which is the displacement angle between the fundamental components of v_p and v_s. If $D_\varphi = \varphi/\pi$ is defined for

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics



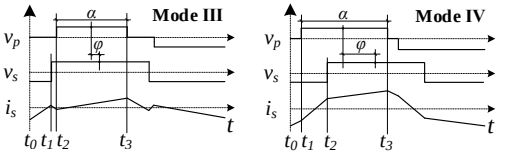
(a) (b)

Fig. 3. (a) typical SPS working waveforms over one switching period, which is a special case of EPS by setting $D_\alpha = 1$ in Mode II (b) the output power P_o and the RMS leakage inductance current $I_{L,rms}$ of the DAB converter with repect to D_φ, $k = 0.75$ in this case.



(a) (b)

Fig. 4. In boost scenario, typical EPS working waveforms in one switching period (a) Mode I, $D_\varphi < (1 - D_\alpha)/2$ (b) Mode II, $D_\varphi > (1 - D_\alpha)/2$.



(a) (b)

Fig. 5. In buck scenario, typical EPS working waveforms in one switching period (a) Mode III, $D_\varphi < (1 - D_\alpha)/2$ (b) Mode IV, $D_\varphi > (1 - D_\alpha)/2$.

simplification, $D_\varphi \in [0, 1]$ stands for forward power flow from V_1 to V_2 and $D_\varphi \in [-1, 0]$ for the reverse direction. In fact, D_φ is often limited in $[-0.5, 0.5]$ to lower the RMS value of the leakage inductance current while maintaining the same power transfer capability, which can be explained by Fig. 3.

Given the SPS working waveforms in Fig. 3(a) and with $T_{sw} = 1/f_{sw}$, the normalized average output power $P_o[pu] = 1/P_b \cdot 1/T_{sw} \cdot \int_0^{T_{sw}} [v_s(t) \cdot i_s(t)]dt$ and the normalized RMS leakage inductance current $I_{s,rms}[pu] = 1/I_b \cdot \sqrt{1/T_{sw} \cdot \int_0^{T_{sw}} i_s^2(t)dt}$ are derived as

$$P_o[pu] = 4kD_\varphi(1 - D_\varphi) \tag{3}$$

$$I_{s,rms}[pu] = \frac{2\sqrt{3}}{3} \cdot \sqrt{(12D_\varphi^2 - 8D_\varphi^3 - 2)k + k^2 + 1} \tag{4}$$

which can be represented by the black curve and red curve in Fig. 3(b), respectively. It can be seen that there are always two points in the ranges of $[0, 0.5]$ and $[0.5, 1]$ for the same power, but the leakage inductance current is smaller in $[0, 0.5]$. This conclusion is also applicable to other phase-shift modulation schemes including EPS.

In EPS, considering the voltage-second balance of the leakage inductor, two operation modes can be found for boost or buck scenario, as shown in Fig. 4 and Fig. 5, respectively. If the inner phase shift is denoted by $D_\alpha = \alpha/\pi$, then $\alpha \in [0, \pi]$ corresponds to $D_\alpha \in [0, 1]$. Clearly, if $D_\alpha = 1$, EPS is fallen into SPS. In this regard, SPS can be seen as a special case of EPS.

The current waveform is shaped by the voltage drop on the leakage inductor.

$$\frac{L}{n^2}\frac{di_s(t)}{dt} = \frac{v_p(t)}{n} - v_s(t) \tag{5}$$

Considering $i_s(t_0) = i_s(t_3)$ in half switching period ($t_3 = T_{sw}/2$), the segmented current can be calculated, as listed in Table I.

In order to achieve zero-voltage switching for all switches, the parasitic capacitor of each off-state transistor should be fully discharged at first, which happens through the resonance of the parasitic capacitor C_{oss} and the leakage inductance

TABLE I
EXPRESSIONS OF THE NORMALIZED LEAKAGE INDUCTANCE CURRENT DURING DIFFERENT INTERVALS FOR EACH EPS OPERATION MODE

Mode I ⇢ Fig. 4(a)	
$[t_0, t_1]$	$i_s(t)[pu] = \frac{8k}{T_{sw}}t - 2k + 2D_\alpha$
$[t_1, t_2]$	$i_s(t)[pu] = \frac{8(k-1)}{T_{sw}}t + 2 - 2k + 4D_\varphi$
$[t_2, t_3]$	$i_s(t)[pu] = \frac{8k}{T_{sw}}t - 2k - 2D_\alpha$
Mode II ⇢ Fig. 4(b)	
$[t_0, t_1]$	$i_s(t)[pu] = \frac{8(k+1)}{T_{sw}}t - 2k - 4D_\varphi + 2$
$[t_1, t_2]$	$i_s(t)[pu] = \frac{8k}{T_{sw}}t - 2k + 2D_\alpha$
$[t_2, t_3]$	$i_s(t)[pu] = \frac{8(k-1)}{T_{sw}}t - 2k + 2 + 4D_\varphi$
Mode III ⇢ Fig. 5(a)	
$[t_0, t_1]$	$i_s(t)[pu] = \frac{8}{T_{sw}}t - (2k-2)D_\alpha - 4D_\varphi$
$[t_1, t_2]$	$i_s(t)[pu] = -\frac{8}{T_{sw}}t - (2k+2)D_\alpha + 4D_\varphi + 4$
$[t_2, t_3]$	$i_s(t)[pu] = \frac{8(k-1)}{T_{sw}}t + (2k-2)D_\alpha + 4D_\varphi + 4 - 4k$
Mode IV ⇢ Fig. 5(b)	
$[t_0, t_1]$	$i_s(t)[pu] = \frac{8}{T_{sw}}t - (2k-2)D_\alpha - 4D_\varphi$
$[t_1, t_2]$	$i_s(t)[pu] = \frac{8(k+1)}{T_{sw}}t + (2k+2)D_\alpha - 4D_\varphi - 4k$
$[t_2, t_3]$	$i_s(t)[pu] = \frac{8(k-1)}{T_{sw}}t + (2k-2)D_\alpha + 4D_\varphi + 4 - 4k$

TABLE II
COMBINED LIMITATIONS BY ZVS AND OPERATIONAL CONSTRAINTS

Mode I	$2k/(1-k)D_\varphi < D_\alpha < k, \quad 0 < D_\varphi < (1-k)/2$
Mode II	$D_\alpha > 2k(1-D_\varphi)/(1+k), \quad (1-k)/2 < D_\varphi < 1/2$
Mode III	$2D_\varphi/(k-1) < D_\alpha < 1/k, \quad 0 < D_\varphi < (k-1)/(2k)$
Mode IV	$D_\alpha > 2(1-D_\varphi)/(1+k), \quad (k-1)/(2k) < D_\varphi < 1/2$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

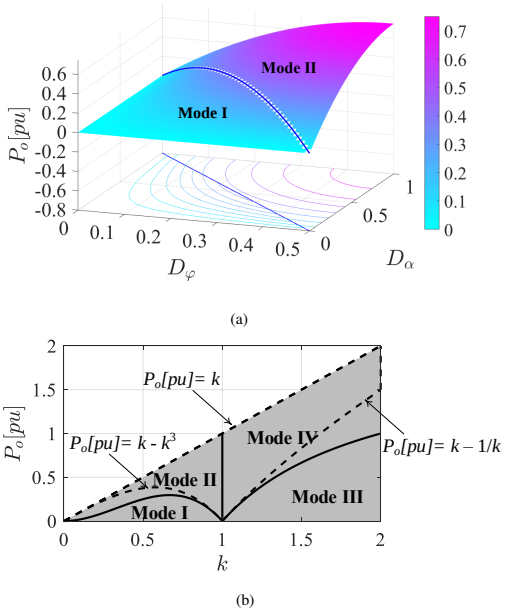


Fig. 6. (a) Output power in terms of D_α and D_φ with the blue curve as the operational constraint. (b) ZVS-limited power transfer range in terms of k: gray area is the ZVS range for EPS and it is divided into 4 parts (i.e. 4 modes) by solid curves. The area encircled by dashed lines is ZVS range for SPS.

L. Afterwards, the body diode will be naturally conducted, resulting in a near-zero source-to-drain voltage V_{DS} (the actual value is equal to the voltage drop on the body diode). Thus zero-voltage switching can be achieved if the transistor is turned on at this moment, indicating that the direction of the current flow is from source to drain at the switching-on instants for $S_1 \sim S_8$. According to this constraint, the polarity of the leakage current at switching instants can be confirmed and the ZVS conditions can be further derived with the current expressions in Table I. Then associating with the operational constraints for each mode, the combined limitations on the control variables are attained in Table II.

C. ZVS-limited Power Transfer Range

Using the current expressions in Table I, the average output power in one switching period can be calculated with

$$P_o[pu] = \begin{cases} 4kD_\alpha D_\varphi & \text{Mode I,III} \\ -k[4D_\varphi^2 - 4D_\varphi + (1-D_\alpha)^2] & \text{Mode II,IV} \end{cases} \tag{6}$$

Since D_φ in I, III is smaller, the power transmission ability is weaker compared to II, IV, as shown in Fig. 6(a). In other words, Mode I and Mode III are suitable for lower power transmission while Mode II and Mode IV for higher. On this basis, the limited power transfer range by considering the ZVS constraints in Table II can be derived as

$$P_o[pu] \in \begin{cases} \left.\begin{matrix} (0, \ \ 2k^2(1-k)] \rightarrow \text{Mode I} \\ (2k^2(1-k), \ \ k] \rightarrow \text{Mode II} \end{matrix}\right\} k<1 \\ \left.\begin{matrix} (0, \ \ 2(k-1)/k] \rightarrow \text{Mode III} \\ (2(k-1)/k, \ \ k] \rightarrow \text{Mode IV} \end{matrix}\right\} k>1 \end{cases} \tag{7}$$

and shown by the gray area in Fig. 6(b). For comparison, in SPS, due to the ZVS conditions $D_\varphi > (1-k)/2$ and $D_\varphi > (k-1)/(2k)$, the power range limited by

$$P_o[pu] \in \begin{cases} [k-k^3, \ \ k] \rightarrow k<1 \\ [k-1/k, \ \ k] \rightarrow k>1 \end{cases} \tag{8}$$

is also plotted in Fig. 6(b). The boundary conditions in (8) are denoted by the dashed lines in Fig. 6(b) . Varying with the voltage ratio k, the ZVS can be theoretically achieved from zero to the maximum power in EPS, while this is applicable to SPS only when $k = 1$. In other words, the ZVS range is considerably extended in EPS because of the introduced control variable D_α.

III. Losses Distribution

A. Transformer and Auxiliary Inductor

The losses of the magnetical components include copper losses and core losses. For the given transformer and inductor in Table III, the copper losses can be calculated with

$$P_{cond,Tr} = \left(\frac{R_L + R_{Trp}}{n^2} + R_{Trs}\right) \cdot I_{s,rms}^2 \tag{9}$$

where R_L is the auxiliary inductor resistance, and R_{Trp}, R_{Trs} are the primary and secondary winding resistances of the transformer, respectively.

For simplification, assuming the transformer and inductor are fed by the fundamental sinusoidal components, this allows for calculating core losses with the Steinmetz equation [39]

$$p_v = C_m f_{sw}^\alpha \hat{B}^\beta \tag{10}$$

and the core volume V_{Tr} and V_L, respectively. The peak magnetic flux density $\hat{B}$ is estimated with $\hat{B}_{Tr} \approx 2V_1/(\pi^2 f_{sw} N_{Trp} A_{Tr})$ (N_{trp}: primary winding turns, A_{Tr}: effective magnetic cross section) and $\hat{B}_L \approx \mu_{eff}\mu_0 N_L \hat{I}_L / l_L$ (μ_{eff}: equivalent relative permeability of a gapped core, N_L: winding turns, $\hat{I}_L$: peak inductor current, l_L: effective magnetic path length) for the transformer and auxiliary inductor, respectively. Detailed information is listed in Table IV.

B. Power Switches

The losses caused by the power semiconductors mainly consist of conduction and switching losses. For the calculation of the conduction losses, the RMS switch currents can be easily derived from the RMS transformer current $I_{s,rms}$ due to that every switch conducts current during half of the switching period. Therefore, given the switch parameters in Table III, he conduction losses of the power switches can be calculated with

$$P_{cond,sw} = 4 \cdot \frac{R_{DSonp}}{N_{swp}} \cdot \left(\frac{I_{s,rms}}{\sqrt{2}n}\right)^2 + 4 \cdot \frac{R_{DSons}}{N_{sws}} \cdot \left(\frac{I_{s,rms}}{\sqrt{2}}\right)^2 \tag{11}$$

TABLE III
COMPONENTS PARAMETERS OF THE IMPLEMENTED PROTOTYPE

Components	Parameters
Primary winding of the DAB HF transformer: 35 turns copper foil	R_{Trp}=607.9 mΩ @T_a=25 ^oC
Secondary winding of the DAB HF transformer: 10 turns copper foil	R_{Trs}=16.5 mΩ @T_a=25 ^oC
Auxiliary inductor: 10 turns Litz wire, 20 strands, 0.355 mm	R_L=27.9 mΩ @T_a=25 ^oC
MOSFETs $S_1 \sim S_4$: IPW65R080CFD	R_{DSonp}=72 mΩ @T_j=25 ^oC
MOSFETs $S_5 \sim S_8$: 2 x IPP110N20N3 in parallel	R_{DSons}=9.6 mΩ @T_j=25 ^oC

TABLE IV
MAGNETIC CORE PARAMETERS

Transformer (core type: ETD59/31/22 material: N97)					
V_{Tr}	A_{Tr}	N_{Trp}	C_m	α	β
51.2 cm^2	368 mm^2	35	8.21	1.28	2.2
Auxiliary Inductor (core type: ETD44/22/15 material: N87)					
V_L	l_L	μ_{eff}	C_m	α	β
17.8 cm^2	10.3 cm	120	10	1.26	2.15

R_{DSonp}/N_{swp} and R_{DSons}/N_{sws} are the equivalent switch on-state resistance if each switch consists of N_{swp} and N_{sws} paralleled semiconductors in the primary and secondary full-bridges, respectively.

On the basis of ZVS turn-on, only turn-off losses are considered for calculating switching losses for each transistor, which can be estimated by [40]

$$p_{sw} = U_{DS} \cdot I_{off} \cdot \frac{t_{ru} + t_{fi}}{2} \cdot f_{sw} \tag{12}$$

where U_{DS} denotes the turn-off voltage and I_{off} is the current at switching-off instants. t_{ru} and t_{fi} are the voltage rise time and current fall time during switching-off transients.

C. Capacitors

The losses dissipated on the input and output capacitors are calculated with the equivalent series resistance (ESR), which can be obtained from the datasheet, leading to

$$p_{cap} = \frac{R_{ESR}}{N_{cap}} I_c^2 \tag{13}$$

where N_{cap} is the number of parallel capacitors. The selected capacitors are one B43544A6397M000 (C_1=0.39 mF) on the input side and five EETEE2D301HJ in parallel (C_2=1.5 mF) on the output side.

D. Losses Distribution

The total losses are the sum of all discussed power losses and can be categorized as switching losses P_{sw}, conduction losses P_{cond}, core losses P_{core} and capacitor losses P_{cap}, namely

$$P_{total} = P_{sw} + P_{cond} + P_{core} + P_{cap} \tag{14}$$

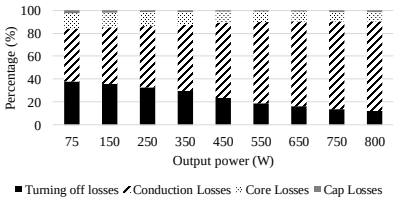


Fig. 7. Calculated losses distribution percentages.

with further specifications:

$$\begin{aligned} P_{sw} &= P_{sw,S_1\sim S_4} + P_{sw,S_5\sim S_8} \\ P_{cond} &= P_{cond,Tr} + P_{cond,sw} \\ P_{core} &= P_{core,Tr} + P_{core,L} \\ P_{cap} &= P_{cap,in} + P_{cap,out} \end{aligned} \tag{15}$$

Operating the converter under ZVS conditions, the calculated losses percentages of different dissipation parts are shown in Fig. 7. It can be seen that for the given setup, the conduction losses are the dominating part over the whole power range, although the switching losses are almost equal to the conduction losses in light load. Besides, the conduction losses portion increases a lot in the heavy load. therefore, reducing conduction losses is of high importance to improve the system performance.

IV. OPTIMIZED MODULATION SCHEMES FOR REDUCING CONDUCTION LOSSES

As shown in Fig. 7, conduction losses are the major loss source for the given converter setup, which are determined by the RMS value of the leakage inductance current $I_{s,rms}$ seen from (9) and (11). It is also shown in (6) that there are infinite combinations of D_α and D_φ for the same average output power, which provides the possibility to reduce the conduction losses without sacrificing other performances. Fig. 8 illustrates an example of operating waveforms with different values of D_α and D_φ but with the same output power. Clearly, the RMS current in Fig. 8(b) is smaller than Fig. 8(a).

As proved in the following, for different output power levels, there exist an optimal operating point at which the leakage inductance current is minimized and simultaneously the ZVS can be guaranteed. But the derived analytical solutions are too complex for practical control. Therefore, a linearized modulation scheme is proposed to simplify the control process.

A. Conventional Current Minimization (OMS1)

The normalized RMS currents $I_{s,rms}[pu]$ for each operation mode are firstly derived based on the working waveforms in Fig. 4 $\sim$ 5, and the results are listed in Table V. In order to minimize the leakage inductance current and satisfy the output power requirements at the same time, the power expression of Mode I in (6) is rewritten as $D_\varphi = P_o[pu]/(4kD_\alpha)$ and then

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

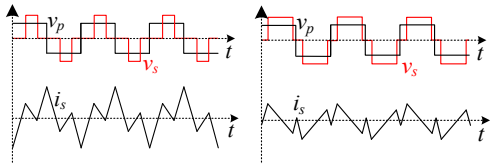


Fig. 8. Simulated working waveforms with different combinations of D_α and D_φ (a) D_α=0.35, D_φ=0.053 (b) D_α=0.73, D_φ=0.026 for the same output power.

TABLE V
EXPRESSIONS OF THE NORMALIZED LEAKAGE INDUCTANCE CURRENT FOR EACH OPERATION MODE

Operation Mode	RMS leakage inductance current $I_{s,\text{rms}}[pu]$
Mode I	$\frac{2}{3}\cdot sqrt\Big[3(k-2)D_\alpha^3+9D_\alpha^2 + (36D_\varphi^2-9)kD_\alpha+3k^2\Big]$
Mode II	$\frac{2}{3}\cdot sqrt\Big[-6D_\alpha^3+(-18kD_\varphi+9k+9)D_\alpha^2 + (36D_\varphi-18)kD_\alpha+3k^2+3k(1-2D_\varphi)^3\Big]$
Mode III	$\frac{2}{3}\cdot sqrt\Big[3-(6k^2-3k)D_\alpha^3+9k^2D_\alpha^2 - 3kD_\alpha(3-12D_\varphi^2)\Big]$
Mode IV	$\frac{2}{3}\cdot sqrt\Big[-6k^2D_\alpha^3+(9k^2-18kD_\varphi+9k)D_\alpha^2 - (18-36D_\varphi)kD_\alpha+3-3(1-2D_\varphi)^3k\Big]$

it is substituted into the expression of $I_{s,rms}[pu]$ in Table V, resulting in

$$I_{s,rms}[pu]= \frac{2}{3}\cdot\sqrt{3(k-2)D_\alpha^3+9D_\alpha^2+\Big(\frac{9P_o[pu]^2}{4k^2D_\alpha^2}-9\Big)kD_\alpha+3k^2} \tag{16}$$

For achieving the extreme value of $I_{s,rms}[pu]$ for a certain output power $P_o[pu]$, the differential of (16) with respect to D_α is set to be 0, namely $\partial I_{s,rms}[pu]/\partial D_\alpha = 0$, solving which will lead to

$$(12k^2-24k)D_\alpha^4+24kD_\alpha^3-12k^2D_\alpha^2-3P_o[pu]^2=0 \tag{17}$$

It is difficult to directly solve for the analytical solution of (17) due to the high order of D_α. So $P_o[pu]$ in (17) is replaced by $4kD_\alpha D_\varphi$, and the simplified result is

$$(k-2)D_\alpha^2+2D_\alpha-k(4D_\varphi^2+1)=0 \tag{18}$$

Then it becomes easy to obtain the solutions of (18), which are

$$D_{\alpha1}=\frac{1-\sqrt{(1-k)^2-4k(2-k)D_\varphi^2}}{2-k} \tag{19}$$

TABLE VI
OPTIMAL VARIABLES RELATIONSHIP WITH MINIMIZED LEAKAGE INDUCTANCE CURRENT IN EACH OPERATION MODE (OMS1)

Mode I --→ Fig. 4(a)
$D_{\alpha,opt1}=\frac{1-\sqrt{(1-k)^2-4k(2-k)D_\varphi^2}}{2-k}, \quad 0<D_\varphi\le\frac{1-k}{2}$
Mode II --→ Fig. 4(b)
$D_{\alpha,opt1}=\frac{2D_\varphi+k-1+\sqrt{(1-k-2D_\varphi)^2+[k(1-2D_\varphi)]^2}}{k}, \quad for \quad \frac{1-k}{2}<D_\varphi<\frac{k-1+\sqrt{1-k^2}}{2k}$
$D_{\alpha,opt1}=1, \quad for \quad \frac{k-1+\sqrt{1-k^2}}{2k}\le D_\varphi<\frac{1}{2}$
Mode III --→ Fig. 5(a)
$D_{\alpha,opt1}=\frac{k-\sqrt{(k-1)^2-4(2k-1)D_\varphi^2}}{2k-1}, \quad 0<D_\varphi\le\frac{k-1}{2k}$
Mode IV --→ Fig. 5(b)
$D_{\alpha,opt1}=kD_\varphi-k+1+\sqrt{[(1-2D_\varphi)k-1]^2+(1-2D_\varphi)^2}, \quad for \quad \frac{k-1}{2k}<D_\varphi<\frac{1-k+\sqrt{k^2-1}}{2}$
$D_{\alpha,opt1}=1, \quad for \quad \frac{1-k+\sqrt{k^2-1}}{2}\le D_\varphi<\frac{1}{2}$

$$D_{\alpha2}=\frac{1+\sqrt{(1-k)^2-4k(2-k)D_\varphi^2}}{2-k} \tag{20}$$

In order to select the correct solution from (19) and (20), the derived ZVS conditions for Mode I (in Table II) are considered. Substituting $D_\varphi<(1-k)/2$ into (19) and (20), the resulted

$$D_{\alpha1}<k \tag{21}$$

$$D_{\alpha2}>(2-2k+k^2)/(2-k)\ge k \tag{22}$$

indicate that $D_{\alpha1}$ satisfies the ZVS condition $D_\alpha<k$ while $D_{\alpha2}$ does not. Therefore, the correct analytical solution of (18) should be $D_{\alpha1}$. In other words, if (19) is satisfied, the leakage inductance current in Mode I for a certain output power will be located at the extreme value point. However, extreme values do not always mean the minimum values.

In order to verify whether $D_{\alpha1}$ is a proper solution of minimal $I_{s,rms}$, the relationships among $I_{s,rms}$-D_α-D_φ (ref. Table V) are depicted in Fig. 9. As shown in Fig. 9(a), only the red-colored area is related to Mode I, limited by the operational condition $D_\alpha<1-2D_\varphi$. It can be seen that for a certain output power, the black intersection points are the minimum $I_{s,rms}[pu]$ at different power levels. Thus it can be concluded that $D_{\alpha1}$ is the correct solution for achieving the minimum $I_{s,rms}$, which is exactly the $D_{\alpha,opt1}$ in Table VI.

Applying similar deriving process to Mode II, the resulting $I_{s,rms}[pu]$ surface with respect to D_α and D_φ is shown in Fig. 9(b). As for Mode III and Mode IV, the optimized results are directly given in Table VI, from which it can be seen that the analytical solution of D_α is segmented depending on the operation range of D_φ in Mode II and Mode IV. Especially,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

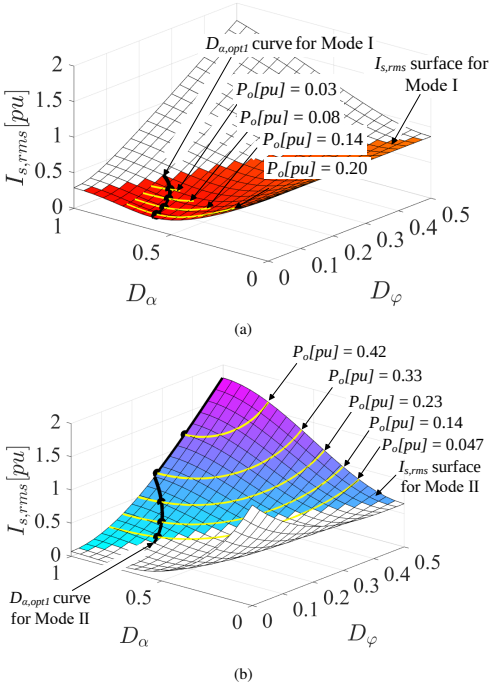


Fig. 9. 3D plot of the RMS leakage inductance current as the function of D_α and D_φ in boost scenario ($k = 0.75$ in this case) for (a) Mode I (b) Mode II. The expressions of $D_{\alpha,opt1}$ for achieving minimum $I_{s,rms}$ at different power levels can be found in Table VI.

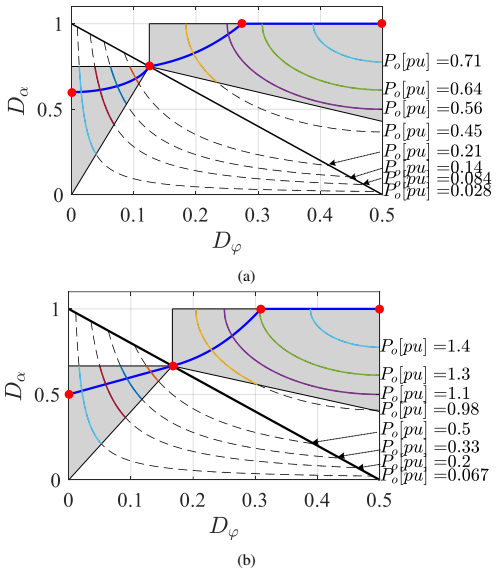


Fig. 10. The relationship function $D_\alpha = f(D_\varphi)$ in OMS1 (denoted by the blue curve) including the gray ZVS range and colored power curves in: (a) Boost scenarios ($k = 0.75$ in this case). (b) Buck scenarios ($k = 1.5$ in this case).

if D_φ is close to 0.5, the optimal D_α is equal to 1, meaning that the DAB converter transfers to the SPS modulation.

The modulation scheme for achieving minimum $I_{s,rms}$ is termed as Optimized Modulation Scheme 1 (OMS1). Although the RMS leakage inductance current can be theoretically minimized by adopting $D_{\alpha,opt1}$, it is difficult to realize OMS1 in practical control due to the complex relationship between D_α and D_φ, as shown in Table VI.

Thus it is important to simplify the relationship expression between D_α and D_φ. Besides D_α and D_φ, the RMS leakage inductance current is also determined by the voltage ratio k (ref. Table V). For different applications, the input and output voltage may change broadly, implying various voltage ratio requirements. On this basis, the following simplifying schemes are optimized considering both conduction losses reduction and different voltage ratio ranges.

B. Simplified Optimal Modulation Schemes

Due to the fact that the OMS1 is hard to realize, it is necessary to simplify the modulation scheme and meanwhile keep $I_{s,rms}$ as close to the minimum value as possible for reducing the conduction losses. As shown in Fig. 10, the gray areas are limited by ZVS conditions and the colored curves denote different output powers. The derived optimal relationship $D_\alpha = f(D_\varphi)$ for minimum $I_{s,rms}$ is represented by the blue curve. Either in buck scenario (Fig. 10(a)) or boost scenario (Fig. 10(b)), there are four key intersections induced by the segmented optimal function, which are shown by the red points. From left to right, the coordinates of these four cross points are derived as $[0, k/(2-k)]$, $[(1-k)/2, k]$, $[(k-1+\sqrt{1-k^2})/(2k), 1]$, $[0.5, 1]$in Fig. 10(a), and $[0, 1/(2k-1)]$, $[(k-1)/(2k), 1/k]$, $[(1-k+\sqrt{k^2-1})/2, 1]$, $[0.5, 1]$ in Fig. 10(b). Since the power is increased with D_φ and D_α, three different load situations are divided by the four intersections, i.e. light load, medium load and heavy load. Based on different voltage ratio requirements and load situations, the $D_{\alpha,opt1}$ expression can be simplified in various ways.

1) Unified Modulation Scheme (OMS2): A unified modulation scheme can be derived by applying curve fitting technique among the three points $[0, 1/(2k-1)]$, $[(k-1)/(2k), 1/k]$ and $[0.5, 1]$, resulting in

$$D_{\alpha.opt2} = \frac{4\,(3k-2)}{k\,(k-2)} D_\varphi^2 + \frac{2\,(2k-1)}{k} D_\varphi + \frac{k}{2-k} \quad (23)$$

which is as proposed in [41]. In this scheme, only one expression is needed over the three load conditions.

Similarly, the unified modulation expression in buck scenarios also can be derived as follows.

$$D_{\alpha,opt2} = \frac{4k(2k-3)}{2k-1} D_\varphi^2 + (4-2k) D_\varphi + \frac{1}{2k-1} \quad (24)$$

The relation expressions denoted by (23) and (24) are plotted as the red curves in Fig. 11. Nevertheless, depending

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

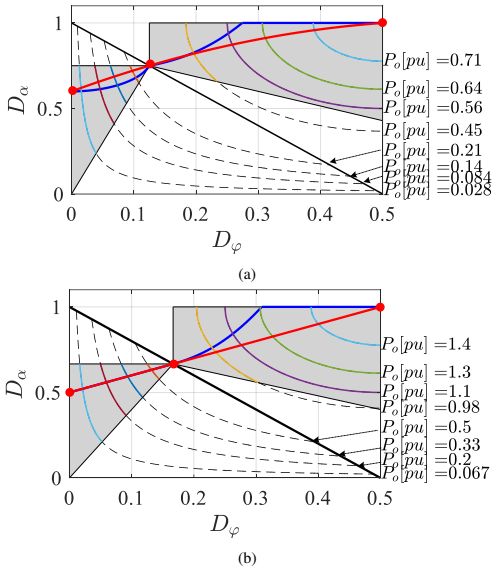


Fig. 11. The relationship function of (a) (23) for Boost scenarios ($k = 0.75$ in this case). (b) (24) for Buck scenarios ($k = 1.5$ in this case) in unified modulation scheme (OMS2), denoted by the red curves.

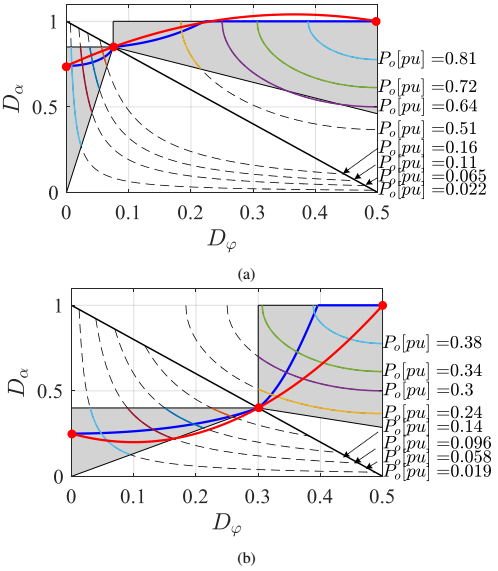


Fig. 12. Two ZVS failure cases for $D_{\alpha,opt2}$ in boost scenarios (a) $k = 0.85$ (b) $k = 0.4$ in unified modulation scheme (OMS2)

on the varying voltage ratio k, the red curve could exceed the gray ZVS range. For example, two failed cases caused by too large or too small k in boost scenarios are shown in Fig. 12, where part of the red curve is beyond the ZVS region. Therefore, there is a limited range of k for unified modulation.

In order to satisfy $D_{\alpha,opt2} \leq 1$ for any value of D_φ in $[0, 0.5]$, the symmetry axis of (23) should be larger than 0.5, then the maximum value of k can be solved, which is

$$\frac{(2k-1)(2-k)}{4(3k-2)} \geq \frac{1}{2} \quad \longrightarrow \quad k_{max} = 0.78 \tag{25}$$

On the other hand, in order to avoid the situation shown in Fig. 12(b), $D_{\alpha,opt2}$ in (23) should be larger than the ZVS border $2kD_\varphi/(1-k)$ for any $D_\varphi \in [0, (1-k)/2]$, leading to

$$\frac{k^2}{2(3k^2-5k+2)} \geq \frac{1-k}{2} \quad \longrightarrow \quad k_{min} = 0.45 \tag{26}$$

Similarly, the k range for (24) can be obtained in the same way, which is within $[1.28, 2.23]$ in buck scenarios for unified modulation scheme.

2) Partially Unified Modulation Scheme (OMS3): Seen from Table VI, EPS transfers into SPS ($D_{\alpha,opt1} = 1$) in heavy load. If the SPS is kept for easy control, the complex optimal expressions in light and medium load can be unified with one expression. In this regard, another group of three points $[0, k/(2-k)]$, $[(1-k)/2, k]$ and $[(k-1+\sqrt{1-k^2})/(2k), 1]$ in boost scenarios are used for curve fitting, and the D_α is kept at 1 in the range of $D_\varphi \in [(k-1+\sqrt{1-k^2})/(2k), 0.5]$. The simplified result will be

$$D_{\alpha,opt3} = \begin{cases} A_k \cdot D_\varphi^2 + B_k \cdot D_\varphi + C_k, \\ \qquad 0 < D_\varphi < \dfrac{k+\sqrt{1-k^2}-1}{2k} \\ 1, \quad \dfrac{k+\sqrt{1-k^2}-1}{2k} \leq D_\varphi \leq \dfrac{1}{2} \end{cases} \tag{27}$$

with

$$\begin{cases} A_k = \dfrac{\left(8-8k-4k^2\right)\sqrt{1-k^2}+8k^3-8k^2-8k+8}{k\,(2-k)\,(1-k^2)} \\ B_k = \dfrac{\left(4-4k-2k^2\right)\sqrt{1-k^2}+2k^3-6k^2-4k+4}{k\,(k+1)\,(k-2)} \\ C_k = \dfrac{k}{2-k} \end{cases} \tag{28}$$

Applying a similar change into the buck scenarios, the curve fitting results are as follows.

$$D_{\alpha,opt3} = \begin{cases} A_k \cdot D_\varphi^2 + B_k \cdot D_\varphi + C_k, \\ \qquad 0 < D_\varphi < \dfrac{1-k+\sqrt{k^2-1}}{2} \\ 1, \quad \dfrac{1-k+\sqrt{k^2-1}}{2} \leq D_\varphi \leq \dfrac{1}{2} \end{cases} \tag{29}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

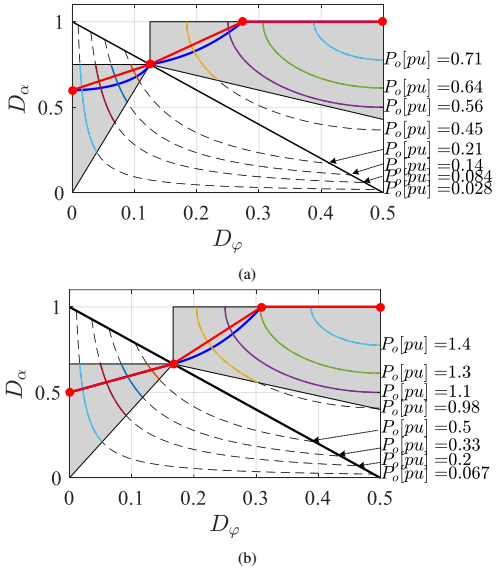


Fig. 13. The linearized relationship function of (a) (31) for Boost scenarios ($k = 0.75$ in this case). (b) (32) for Buck scenarios ($k = 1.5$ in this case) in linear modulation scheme (OMS4), denoted by the red curves.

with

$$\begin{cases} A_k = \dfrac{4k[(2k^2-2k-1)\sqrt{k^2-1}+2(k+1)(k-1)^2]}{2k^3-k^2-2k+1} \\ B_k = \dfrac{(4k+2-4k^2)\sqrt{k^2-1}-4k^3+4k^2+6k-2}{2k^2+k-1} \\ C_k = \dfrac{1}{2k-1} \end{cases} \tag{30}$$

Similar to the unified modulation scheme (OMS1), the voltage ratio in (27) and (29) needs to be limited within $[0.56, 0.91]$ and $[1.10, 1.80]$, respectively.

3) Linearized Modulation Scheme (OMS4): One common drawback of OMS2 and OMS3 is the limited range of voltage ratio k. In order to overcome this, a piecewise linear approximation scheme can be derived by considering the three load situations individually. Therefore, the four key points are all taken into account to linearize the complex exressions in Table VI, resulting in

$$D_{\alpha,opt4} = \begin{cases} \frac{2k}{2-k}D_\varphi + \frac{k}{2-k}, & D_\varphi \in [0, \frac{1-k}{2}] \\ \frac{(2-2k^2+2\sqrt{1-k^2})}{k(1+k)}D_\varphi - \frac{(1-k)\sqrt{1-k^2}+1-k-2k^2}{k(1+k)}, & D_\varphi \in [\frac{1-k}{2}, \frac{k-1+\sqrt{1-k^2}}{2k}] \\ 1, & D_\varphi \in [\frac{k-1+\sqrt{1-k^2}}{2k}, 0.5] \end{cases} \tag{31}$$

in boost scenarios and

$$D_{\alpha,opt4} = \begin{cases} \frac{2}{2k-1}D_\varphi + \frac{1}{2k-1}, & D_\varphi \in [0, \frac{k-1}{2k}] \\ \frac{2k\sqrt{k^2-1}+2k^2-2}{k+1}D_\varphi - \frac{(k-1)\sqrt{k^2-1}+k^2-k-2}{k+1}, & D_\varphi \in [\frac{k-1}{2k}, \frac{1-k+\sqrt{k^2-1}}{2}] \\ 1, & D_\varphi \in [\frac{1-k+\sqrt{k^2-1}}{2}, 0.5] \end{cases} \tag{32}$$

in buck scenarios.

Fig. 13 gives two cases derived from (31) and (32), respectively. It can be clearly seen that no matter how the voltage ratio changes, the linearized red curves will always locate within the gray ZVS area. Accordingly, the linerized modulation scheme (OMS4) is set free from the voltage ratio limitation.

C. Comparison of Different Optimized Schemes

Based on different voltage ratio requirements and the preferred working conditions of the converter, the approximation principles of OMS2 $\sim$ OMS4 have been explained in Section IV-B. Compared to the original OMS1 in Section IV, the three simplified schemes have their own pros and cons. In the following, a detailed comparison will be performed from different perspectives.

Firstly, with regard to the unification (depending on D_φ), it can be evaluated by the number of segments in the relationship functions between D_α and D_φ, which is represented by the stars number in the second column of Table VII. More segments means poorer unification performance. Although both OMS1 and OMS4 have the same three segments, the OMS4 is easier to implement due to the linear approximation.

Then the voltage ratio limitations (i.e. k range) are compared for different schemes. As shown in last section, OMS1 and OMS4 can theoretically guarantee ZVS for any value of k, whereas a limited range should be considered for OMS2 and OMS3 to avoid ZVS failure over the whole power transfer range. In this regard, OMS1, OMS4 are better than OMS2, OMS3.

From the point of calculation burden, two conditions of the voltage ratio are considered, i.e. a fixed or a varying k. If V_1 and V_2 are fixed, the voltage ratio can be seen as a constant and thereby the $k-$depending coefficients (e.g. A_k, B_k, C_k) of $D_{\alpha,opti}(i = 1, 2, 3, 4)$ expressions are also constants. On this basis, $D_{\alpha,opt4}$ has the simplest form due to the lower number of mathematical multiplications and square roots, which also means faster processing speed for the digital processor. This advantage will become further clear when multiple DAB modules are working at the same time. On the other hand, if V_1 and V_2 are varying, the sampling speed of V_1, V_2 and the calculation burden of the $k-$depending coefficients should be taken into account. Regarding this, it can be found that OMS2 surpasses the other schemes, represented by four stars in Table VII.

At last, assuming the converter works in steady sate, the input and output voltages are stabilized with a fixed k. In respect of this, the complexity of different schemes are evaluated by adding the star numbers from the second to fourth column in

TABLE VII
COMPARISON OF OMS1, OMS2, OMS3 AND OMS4

	Unification	Voltage limitation	Calculation burden		Complexity
			fixed k	varying k	
OMS1	★	★★	★	★	4 · ★
OMS2	★★★	★	★★	★★★★	6 · ★
OMS3	★★	★	★★★	★★	6 · ★
OMS4	★	★★	★★★★	★★★	7 · ★

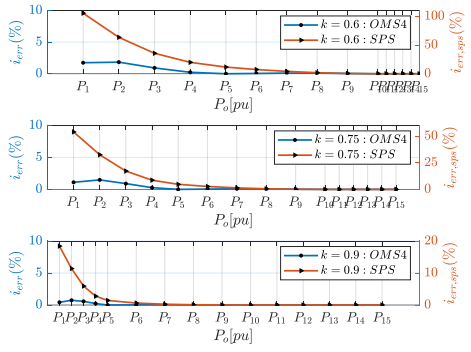


Fig. 14. Relative errors defined by (33) varying with voltage ratios and output powers

Table VII, and the summations are shown in the last column. It can be seen that OMS has the highest 7 stars, and thus will be selected as the focus to further evaluate the effectiveness on reducing conduction losses.

V. RESULTS AND DISCUSSION

As illustrated in IV-C, the linearized modulation scheme (OMS4) overtakes other schemes with a simpler form of modulation expression. However, OMS4 is essentially an approximating method, and this means that the effectiveness on conduction losses reduction is not as good as OMS1 which can achieve minimum leakage inductance current $I_{s,rms}$. Hence the relative error calculated by (33) is used to measure the deviation from the minimum $I_{s,rms}$.

$$i_{err} = \frac{|I_{s,rms,OMS4} - I_{s,rms,OMS1}|}{I_{s,rms,OMS1}} \cdot 100\% \qquad (33)$$

For comparison, the values of $I_{s,rms}$ under SPS modulation is also calculated, and the following relative error between $I_{s,rms,sps}$ and the minimum $I_{s,rms,OMS1}$ is used to compare with (33).

$$i_{err,sps} = \frac{|I_{s,rms,sps} - I_{s,rms,OMS1}|}{I_{s,rms,OMS1}} \cdot 100\% \qquad (34)$$

The calculated results varying with different voltage ratios and normalized output powers are shown in Fig. 14. Therein,

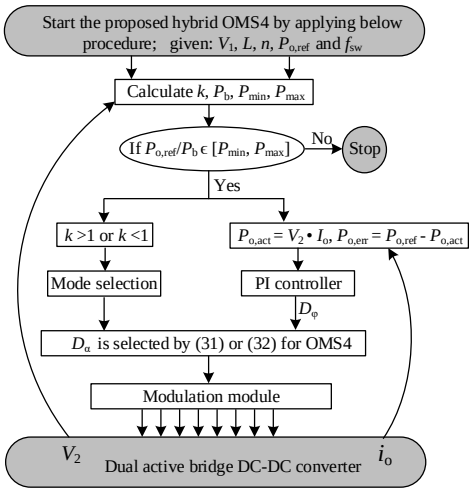


Fig. 15. Procedure of applying linearized modulation scheme (OMS4) to the DAB converter

P_5, P_{10} and P_{15} are the $k-$related output powers at the three boundary points (i.e. $[(1-k)/2, k]$, $[(k-1+\sqrt{1-k^2})/(2k), 1]$, $[0.5, 1]$ that define the three segments in OMS4 in boost scenarios). Then the various other power levels $P_i (i = 1..15)$ can be expressed by

$$P_i = \begin{cases} 0.2 \cdot i \cdot P_5, & i = 1..5 \\ P_5 + 0.2 \cdot (i-5) \cdot (P_{10} - P_5), & i = 6..10 \\ P_{10} + 0.2 \cdot (i-10) \cdot (P_{15} - P_{10}), & i = 11..15 \end{cases} \qquad (35)$$

with

$$P_5 = 2k^2(1-k), P_{10} = \frac{2(k^2 - 1 + \sqrt{1-k^2})}{k}, P_{15} = k \qquad (36)$$

From Fig. 14, it can be seen that $i_{err,sps}$ is larger than $i_{err,OMS4}$, especially in light load and medium load. When the voltage ratio k is 0.6, the maximum $i_{err,sps}$ even exceeds 100%. Consequently, it can be obtained that OMS4 is more applicable to the DAB converter, especially when the converter works in light load and the voltage ratio deviates far from unity. On the other hand, comparing $I_{s,rms,OMS4}$ with the optimal $I_{s,rms,OMS1}$, the relatives errors i_{err} are very small (less than 2%) for various voltage ratios and output power levels, especially in medium and high power load ($P_5 \sim P_{15}$, less than 0.5%), which proves the effectiveness of linearized modulation scheme on reducing the conduction losses. The process of applying OMS4 to the DAB converter is illustrated in Fig. 15.

An experimental platform for the DAB converter is built to validate the linearized modulation scheme OMS4, as shown in Fig. 16. The main circuit parameters are listed in Table VIII.

In order to fully evaluate the performance improvement caused by linearized modulation scheme, two groups of com-

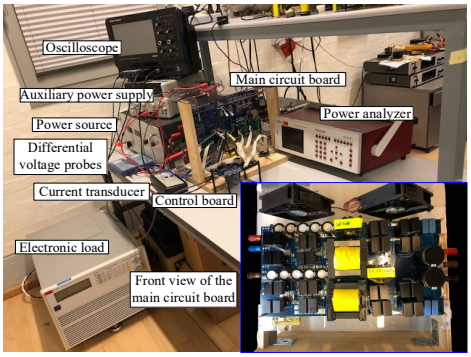


Fig. 16. Test platform for the DAB converter

TABLE VIII
SYSTEM SPECIFICATIONS

Parameters	Description	Value
P	Rating power	1.5 kW
$n:1$	Turns ratio of the transformer	3.5 : 1
f_{sw}	Switching frequency	60 kHz
T_{dead}	Dead time	400 ns
L_s	Series inductor	36.2 μH
L_{trp}	Primary-side leakage inductance	4.5 μH
L_{trs}	Secondary-side leakage inductance	372.5 nH
C_1	Primary DC capacitor	0.78 mF
C_2	Secondary DC capacitor	1.5 mF

parative experiments are conducted for each mode: group one (G1) adopts the optimized linear modulation (OMS4) and the other group (G2) does not use any optimized scheme (but still modulated by EPS). Moreover, for the purpose of highlighting the effect of the conduction losses, the operating points of two groups are both located within the ZVS range. As shown in IV-B3, the piecewise linear scheme has three segments. Therefore, for either boost or buck scenarios, the measured working waveforms with three different output power levels are shown in the following.

In Mode I, the steady state waveforms of the DAB converter are illustrated in Fig. 17, where v_p and v_s are voltage waveforms generated by HB_1 and HB_2, and i_p, i_s are the primary and secondary transformer current, respectively. Fig. 17(a) shows the measured waveforms when the DAB converter works without adopting any optimized modulation (belongs to G2). Fig. 17(b) shows the working waveforms when the converter is modulated by linearized scheme (belongs to G1). The output power for both situations is given at 190 W. As marked in the figure, the value of $I_{s.rms}$ in Fig. 17(b) is lower than that in Fig. 17(a), indicating the effectiveness of OMS4 in reducing the conduction losses of the DAB converter. As a result, the overall system efficiency is improved from 92.5% to 95 %. Besides, in order to directly see if the ZVS is achieved, the drain-source voltage and the gate signal of S_7 (turned on at the rising edge of v_s) are illustrated in Fig. 17(c) and Fig.

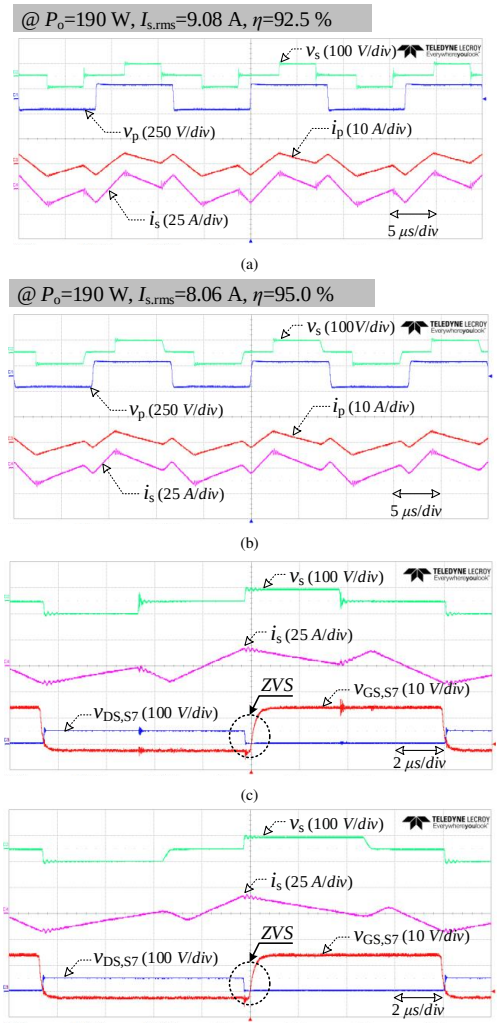


Fig. 17. Experimental waveforms of DAB converter in Mode I where V_1=120 V, V_2=46 V ($k = 0.75$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

17(d), corresponding to the working conditions in Fig. 17(a) and Fig. 17(b), respectively. It can be seen that the switching-on signal (i.e. rising edge) of $v_{GS,S7}$ comes after the drain-source voltage $v_{DS,S7}$ becoming zero, which implies that the transistor S_7 has achieved zero-voltage turn-on.

In Mode II, the converter is operated at two power levels (i.e. 430 W and 700 W) and the working waveforms are shown in Fig. 18 and Fig. 19, respectively. Although there

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

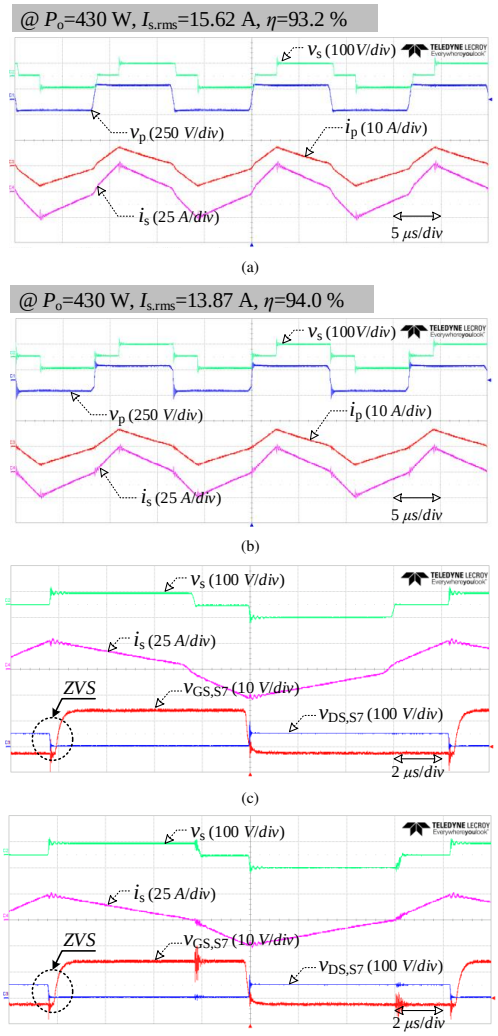


Fig. 18. Experimental waveforms of DAB converter in Mode II where V_1=120 V, V_2=46 V ($k = 0.75$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

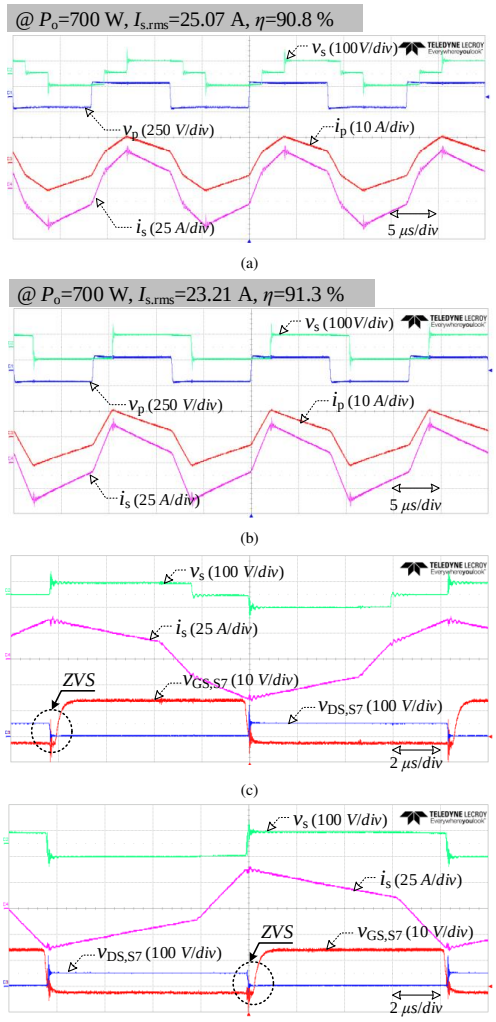


Fig. 19. Experimental waveforms of DAB converter in Mode II where V_1=120 V, V_2=46 V ($k = 0.75$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

are some oscillations at the switching-on instants of S_7, the voltage across S_7 is kept at zero when the gate signal reaches high level, thus ZVS is still guaranteed in these two higher power situations. On the other hand, compared to Fig. 18(a) and Fig. 19(a), the converter efficiency is improved when the optimized linear modulation scheme is utilized in Fig. 18(b) and Fig. 19(b), respectively.

In terms of buck scenarios, Fig. 20 $\sim$ Fig. 22 present the corresponding waveforms for Mode III and Mode IV, respectively. Similar conclusions can be achieved with reduced conduction losses and improved efficiency. Also, the ZVS is realized at different output power levels.

Besides, the linear OMS4 is essentially a hybrid modulation scheme, consisting of EPS in light, medium load and SPS in heavy load. This can be seen from the expressions (31) and (32) and the working waveforms in Fig. 19 and Fig. 22. By switching the converter between light load and heavy load with

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

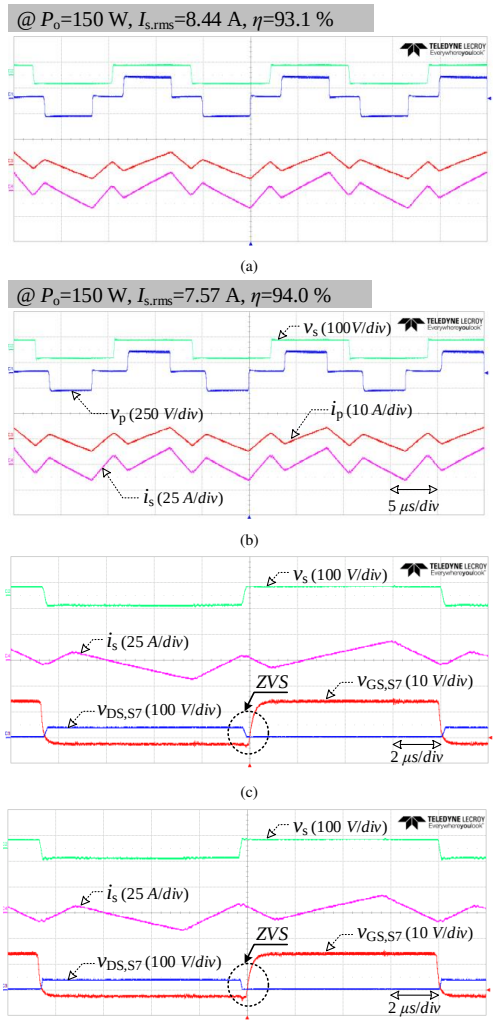


Fig. 20. Experimental waveforms of DAB converter in Mode III where V_1=190 V, V_2=36 V ($k = 1.5$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

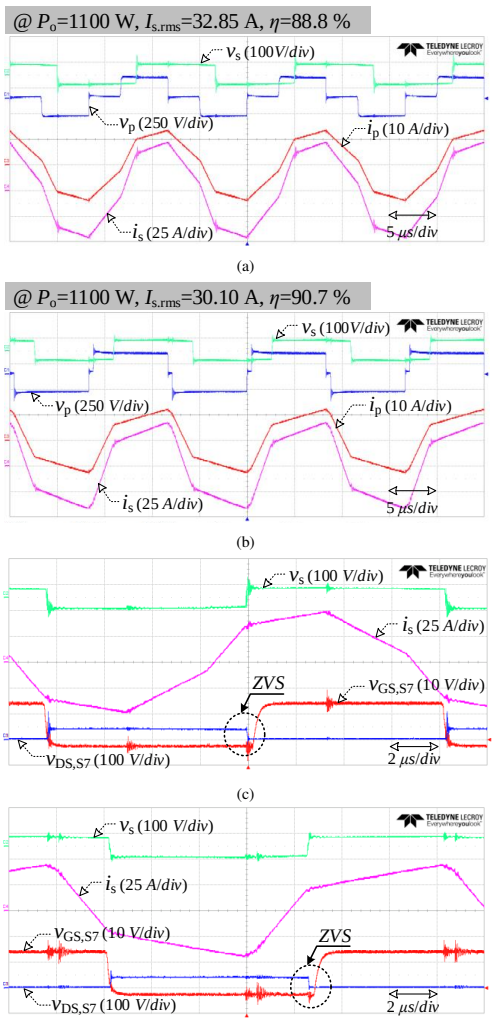


Fig. 21. Experimental waveforms of DAB converter in Mode IV where V_1=190 V, V_2=36 V ($k = 1.5$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

OMS4, the dynamic response is shown in Fig. 23, where V_2 is the output dc voltage, i_o is the output current and i_s is the leakage inductance current referred to the secondary side. The power is increased from 150 W to 700 W in Fig. 23(a) and then decreased in Fig. 23(b). Part of i_s is amplified in green frames for having a clear view on the current shape of i_s. It can be seen that the converter can smoothly changes from EPS to SPS or reverse depending on the power condition.

Furthermore, the input and output voltage are changed to operate the converter with different voltage ratios, and the measured efficiency curves are shown in Fig. 24. Corresponding to boost and buck scenarios, Fig. 24(a) ($k = 0.9$) and Fig. 24(b) ($k = 1.2$) plot the converter efficiency at different output powers. In the figure, three situations are illustrated: the red curve denotes the linearized modulation scheme (belongs to G1), the blue curve represents the normal EPS modulation without any optimization (belongs to G2) and the black curve

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2956323, IEEE Journal of Emerging and Selected Topics in Power Electronics

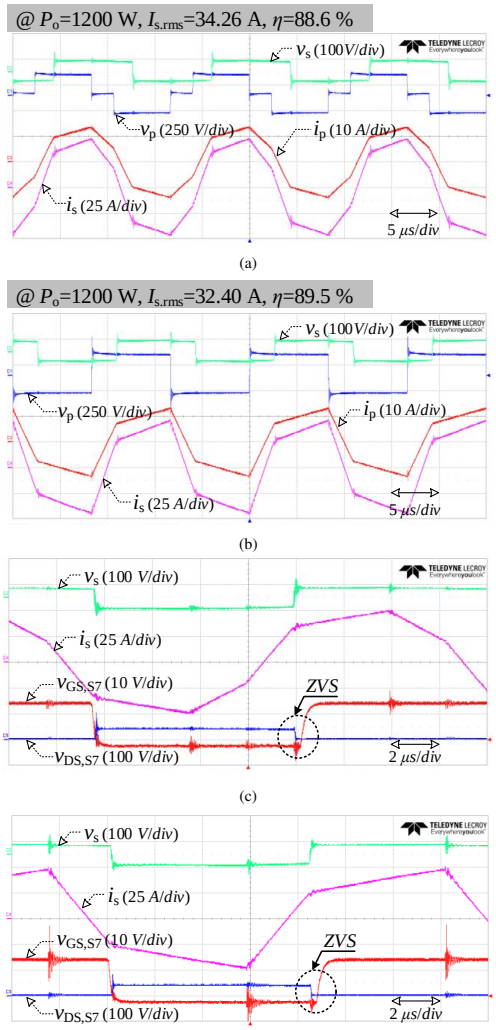


Fig. 22. Experimental waveforms of DAB converter in Mode III where V_1=190 V, V_2=36 V ($k = 1.5$) (a) working waveforms without optimized modulation (b) working waveforms with linearized modulation scheme (c) ZVS realization without optimized modulation (d) ZVS realization with linearized modulation scheme.

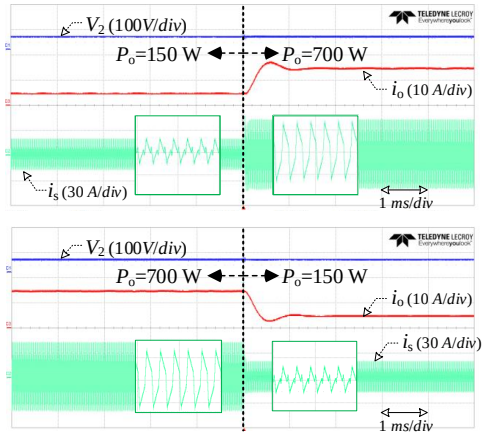


Fig. 23. Dynamic response with the output power (a) increased from 150 W to 700 W (b) decreased from 700 W to 150 W in boost scenario (V_1=120 V, V_2=46 V).

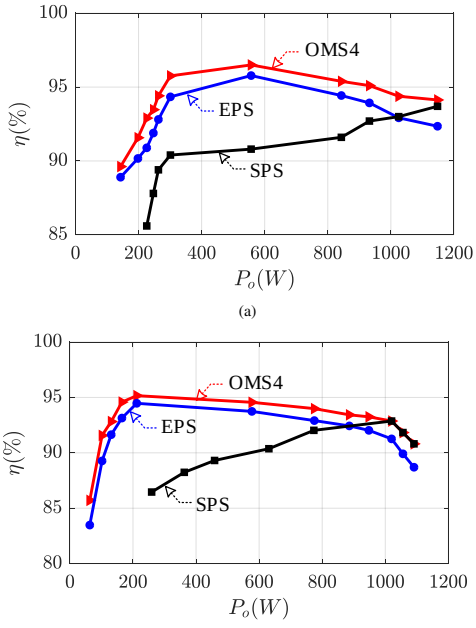


Fig. 24. Measured efficiency curves of the DAB converter for different output power levels, where the red curve, blue curve and black curve denote the converter efficiencies with linear modulation scheme (G1), without any optimization (G2) and with SPS, respectively. (a) Boost operation, V_1=190 V, V_2=60 V ($k = 0.9$) (b) Buck operation, V_1=190 V, V_2=45 V ($k = 1.2$).

is the resulted efficiency by applying SPS over the whole power range. Among the three situations, the linearized modulation scheme has a better efficiency performance in either boost or buck scenarios. In light load, due to the ZVS failure in SPS (black curve), the induced switching losses result in lower efficiency compared to the other two situations (G1 and G2). When the converter works with higher output power, the linearized modulation transfer into SPS scheme and thus the red curve and the black curve are overlapped in heavy load

conditions. In terms of G2 (blue curve), since it can also achieve ZVS, the efficiency is higher than SPS in light and medium load, but lower than G1 because of the larger leakage inductance current.

VI. Conclusions

In order to reduce the conduction losses of the DAB converter and still keep other performance parameters unchanged, an optimized hybrid modulation scheme is proposed in this paper. On the basis of achieving ZVS over the whole operation range and maintaining the same power transfer ability as the single phase shift modulation, an optimal modulation scheme is firstly derived with minimum leakage inductance current. By exploring the possibility to further simplify the relationship functions between the control variables, three other modulation schemes are presented considering various voltage ratio requirements and working conditions for the DAB converter. Therein, the linearized modulation scheme is prominent with less complexity after a through comparative analysis and thus is selected as the focus of this paper. By operating the converter with linear modulation scheme, the conduction losses can be effectively reduced and the system efficiency is improved. Comparative experiments are implemented to highlight the conduction losses reduction and in addition, the experimental results also validate the ZVS realization with linear modulation.

References

[1] R. D. Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high power density DC/DC converter for high power applications," in *Conference Record of the 1988 IEEE Industry Applications Society Annual Meeting*, IEEE, 1988.

[2] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC–DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, 2012.

[3] S. Inoue and H. Akagi, "A bidirectional DC–DC converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, 2007.

[4] X. Wang, F. Tian, and I. Batarseh, "High efficiency parallel post regulator for wide range input DC–dc converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 852–858, Mar. 2008.

[5] J. Biela, U. Badstuebner, and J. W. Kolar, "Impact of power density maximization on efficiency of DC–dc converter systems," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 288–300, Jan. 2009.

[6] N. M. L. Tan, N. M. L. Tan, S. Inoue, S. Inoue, A. Kobayashi, and H. Akagi, "Voltage balancing of a 320-V, 12-F electric double-layer capacitor bank combined with a 10-kW bidirectional isolated DC–DC converter," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2755–2765, Nov. 2008.

[7] M. B. Camara, H. Gualous, F. Gustin, A. Berthon, and B. Dakyo, "DC/dc converter design for supercapacitor and battery power management in hybrid vehicle applications—polynomial control strategy," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 587–597, Feb. 2010.

[8] F. Z. Peng, and J. S. Lawler, "A new ZVS bidirectional DC-dc converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[9] R. T. Naayagi, A. J. Forsyth, and R. Shuttleworth, "High-power bidirectional DC–dc converter for aerospace applications," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4366–4379, Nov. 2012.

[10] Z. Wang, B. Liu, L. Guan, Y. Zhang, M. Cheng, B. Zhang, and L. Xu, "A dual-channel magnetically integrated EV chargers based on double-stator-winding permanent-magnet synchronous machines," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1941–1953, Mar. 2019.

[11] Z. Wang, B. Liu, Y. Zhang, M. Cheng, K. Chu, and L. Xu, "The chaotic-based control of three-port isolated bidirectional dc/dc converters for electric and hybrid vehicles," *Energies*, vol. 9, no. 2, p. 83, 2016.

[12] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC–dc converters using novel dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.

[13] H. Wu, Y. Lu, T. Mu, and Y. Xing, "A family of soft-switching DC–dc converters based on a phase-shift-controlled active boost rectifier," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 657–667, Feb. 2015.

[14] G. Xu, D. Sha, Y. Xu, and X. Liao, "Hybrid-bridge-based DAB converter with voltage match control for wide voltage conversion gain application," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1378–1388, Feb. 2018.

[15] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift control of isolated bidirectional DC–dc converter for power distribution in microgrid," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4667–4680, Nov. 2012.

[16] F. Li, Y. Li, and X. You, "Optimal dual-phase-shift control strategy of an isolated buck–boost converter with a clamped inductor," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5374–5385, Jun. 2018.

[17] B. Liu, P. Davari, and F. Blaabjerg, "A flexible control scheme for single-stage DAB AC/DC converters," in *Proc. IEEE Int. Power Electronics and Application Conf. and Exposition (PEAC)*, Nov. 2018, pp. 1–6.

[18] X. Liu, Z. Q. Zhu, D. A. Stone, M. P. Foster, W. Q. Chu, I. Urquhart, and J. Greenough, "Novel dual-phase-shift control with bidirectional inner phase shifts for a dual-active-bridge converter having low surge current and stable power control," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 4095–4106, May 2017.

[19] G. Xu, D. Sha, J. Zhang, and X. Liao, "Unified boundary trapezoidal modulation control utilizing fixed duty cycle compensation and magnetizing current design for dual active bridge DC–dc converter," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2243–2252, Mar. 2017.

[20] B. Liu, P. Davari, and F. Blaabjerg, "An optimized control scheme to reduce the backflow power and peak current in dual active bridge converters," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, 2019, pp. 1622–1628.

[21] C. Calderon, A. Barrado, A. Rodriguez, P. Alou, A. Lazaro, C. Fernandez, and P. Zumel, "General analysis of switching modes in a dual active bridge with triple phase shift modulation," *Energies*, vol. 11, no. 9, p. 2419, 2018.

[22] O. M. Hebala, A. A. Aboushady, K. H. Ahmed, and I. Abdelsalam, "Generic closed-loop controller for power regulation in dual active bridge DC–dc converter with current stress minimization," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4468–4478, Jun. 2019.

[23] B. Zhao, Q. Song, W. Liu, and W. Sun, "Current-stress-optimized switching strategy of isolated bidirectional DC–dc converter with dual-phase-shift control," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4458–4467, Oct. 2013.

[24] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified triple-phase-shift control to minimize current stress and achieve full soft-switching of isolated bidirectional DC–dc converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.

[25] N. Hou, W. Song, and M. Wu, "Minimum-current-stress scheme of dual active bridge DC–dc converter with unified phase-shift control," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8552–8561, Dec. 2016.

[26] Q. Gu, L. Yuan, J. Nie, J. Sun, and Z. Zhao, "Current stress minimization of dual-active-bridge DC–dc converter within the whole operating range," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 129–142, Mar. 2019.

[27] H. Shi, H. Wen, J. Chen, Y. Hu, L. Jiang, G. Chen, and J. Ma, "Minimum-backflow-power scheme of DAB-based solid-state transformer with extended-phase-shift control," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3483–3496, Jul. 2018.

[28] H. Wen, W. Xiao, and B. Su, "Nonactive power loss minimization in a bidirectional isolated DC–dc converter for distributed power systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6822–6831, Dec. 2014.

[29] A. Tong, L. Hang, G. Li, X. Jiang, and S. Gao, "Modeling and analysis of a dual-active-bridge-isolated bidirectional DC/dc converter to minimize RMS current with whole operating range," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5302–5316, Jun. 2018.

[30] S. Chakraborty and S. Chattopadhyay, "Minimum-RMS-current operation of asymmetric dual active half-bridge converters with and without ZVS," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5132–5145, Jul. 2017.

[31] W. Choi, K. Rho, and B. Cho, "Fundamental duty modulation of dual-active-bridge converter for wide-range operation," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4048–4064, Jun. 2016.

[32] G. G. Oggier and M. Ordonez, "High-efficiency DAB converter using switching sequences and burst mode," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2069–2082, Mar. 2016.

[33] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[34] H. Zhou and A. M. Khambadkone, "Hybrid modulation for dual-active-bridge bidirectional converter with extended power range for ultracapacitor application," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1434–1442, Jul. 2009.

[35] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal ZVS modulation of single-phase single-stage bidirectional DAB AC–dc converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3954–3970, Aug. 2014.

[36] J. Hiltunen, V. Väisänen, R. Juntunen, and P. Silventoinen, "Variable-frequency phase shift modulation of a dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7138–7148, Dec. 2015.

[37] H. Akagi, T. Yamagishi, N. M. L. Tan, S. Kinouchi, Y. Miyazaki, and M. Koyama, "Power-loss breakdown of a 750-V 100-kW 20-kHz bidirectional isolated DC–dc converter using SiC-MOSFET/sbd dual modules," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 420–428, Jan. 2015.

[38] T. Cappello, A. Santarelli, and C. Florian, "Dynamic ron characterization technique for the evaluation of thermal and off-state voltage stress of GaN switches," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3386–3398, Apr. 2018.

[39] W. A. Roshen, "A practical, accurate and very general core loss model for nonsinusoidal waveforms," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 30–40, Jan. 2007.

[40] M. P. D. Graovac and A. Kiep, "Mosfet power losses calculation using the datasheet parameters," Available online at https://www.infineon.com, Tech. Rep., 2008.

[41] B. Liu, P. Davari, and F. Blaabjerg, "An optimized control scheme for reducing conduction and switching losses in dual active bridge converters," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 622–629.

Journal publication 2

Nonlinear Coss-VDS Profile based ZVS Range Calculation for Dual Active Bridge Converters [J2]

B. Liu, P. Davari and F. Blaabjerg

The paper has been published in
IEEE Trans. Power Electron., Early Access, 2020.

The layout has been revised.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.3003248, IEEE Transactions on Power Electronics

Nonlinear C_{oss}-V_{DS} Profile based ZVS Range Calculation for Dual Active Bridge Converters

Bochen Liu, *Student Member, IEEE,* Pooya Davari, *Senior Member, IEEE,* Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—Generally, power electronic converters are designed to obtain the highest efficiency at rated power while they are most often operated under partial loading conditions. For dual active bridge (DAB) converters, the zero-voltage-switching (ZVS) conditions can be impaired under light load situations. While load depending ZVS operation has been introduced by prior-art approaches, the nonlinear characteristic of the output capacitance in a power device is often not considered and its effect on operating boundaries of ZVS is neglected. In this letter, based on practical switching transients, an improved method of calculating the ZVS range is introduced. By taking into account the non-linearity of output capacitance, the method is developed from a detailed analysis of real switching transients. A 2.5 kW prototype is built, and a comprehensive comparison with prior-art approaches is conducted to validate the accuracy of the proposed method.**

I. Introduction

One advantage of the DAB converter [1] is the inherent capability of naturally achieving ZVS for all switches without any auxiliary circuits, and this advantage has facilitated a wide application of DAB converters, such as in distributed power systems [2], energy storage systems [3] and electric vehicles [4]. However, due to the lower leakage inductance current in light-load conditions, the charge stored in the transistor output capacitor may not be totally released during the dead time, and this might result in ZVS failure owing to high voltage across the transistor at the turn-on instant. This failure would further increase the switching losses, impair the electromagnetic compatibility (EMC) performance [5] and even damage the power devices [6].

There are two commonly used methods to identify the limitations on the control variables for achieving ZVS, i.e. current-based method [7], [8] and energy-based method [9]. Therein, the current-based method is developed from the body diode conduction when the power device is switched on and thus ZVS conditions can be attained by controlling a positive or negative leakage inductance current at the switching instants. However, the positive/negative current direction is the result of the ZVS achievement, which is not sufficient to guarantee a soft switching. In respect to the energy-based method, the ZVS is achieved under the condition that the energy stored in the output capacitance C_{oss} is totally released before the transistor is switched on. This method is better by requiring a minimum leakage inductance current at the switching instants. However, the non-linearity of the parasitic output capacitance is usually not taken into account, in spite of the fact that the output capacitance of a power device varies a lot during the turn-on/turn-off procedure. Besides, the calculation procedure is complex regarding the square mathematical operation of the stored energy(e.g. $1/2Li^2$). Moreover, due to that more converter components are involved in the calculation, a high modeling accuracy of the involved components (e.g. the transformer) is required for an accurate ZVS range calculation and this accurate modeling would further increase the complexity. Consequently, owing to the missing consideration of the non-linearity and the complex calculation procedure, the obtained ZVS range using the method would contain some critical operating points that could lead to ZVS failure.

A charge-based ZVS calculation method is proposed in [10], where the nonlinear change of output capacitance is involved. This method can achieve a more accurate ZVS operating range, and thus this letter also calculates the ZVS range based on the charge balance. But compared to the method in [10], the main difference and improvements of the proposed method in this letter are listed in the following.

Firstly, the calculation of the available charges in [10] is not appropriate. In [10], the integration of the bridge current starts from the zero-crossing time instants to the switching moment, and the results are compared with the required discharge of the output capacitance. However, the time range between the two zero-crossing instants [10] might not be the discharging time interval of the output capacitance. In practical switching transients (cf. Section II), the actual integration limits should start from the instant when the drain-source voltage begin to reduce, and end at the instant when the drain-source voltage becomes zero. The whole discharging interval is within this starting point and ending point, during which the discharge of the output capacitance synchronizes with the charge movement in the bridge current. Hence, this discharging interval is the proper integration interval for calculating the conveyed charges by the bridge current. Actually, this discharging interval is equal to the dead time, and it is not involved in the charge calculation in [10]. More details can be found in Section IV.

Secondly, the half dc-bus voltage change consideration in [10] is not appropriate because the drain-source voltage of a power device will switch between zero and the whole dc-bus voltage during transients. The turn-on of one power device corresponds to the turn-off of the other one at the same time. Therefore, the charge and discharge of the power devices in the same bridge leg are analyzed together (Section III) in this paper.

In this letter, a nonlinear C_{oss} profile based ZVS range calculation method is presented according to practical switching transients in a DAB converter. Notably, this method can be applied to the full load range, but due to that the DAB is easier to lose ZVS in light load, this letter will focus on light-load operation. The measured switching transients are

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.3003248, IEEE Transactions on Power Electronics

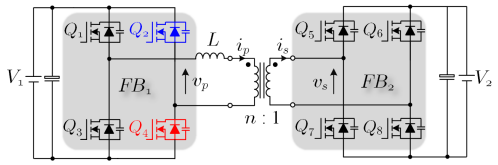


Fig. 1. Circuit topology of a DAB converter with full-bridges FB_1 and FB_2.

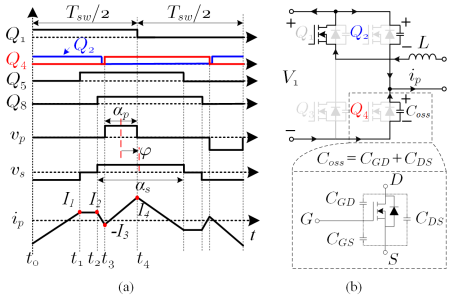


Fig. 2. Operation of the DAB converter (a) Typical operation mode characterized by α_p, α_s and φ. (b) General MOSFET model and resultant circuit state of the full-bridge FB_1 during the turn-on of Q_4.

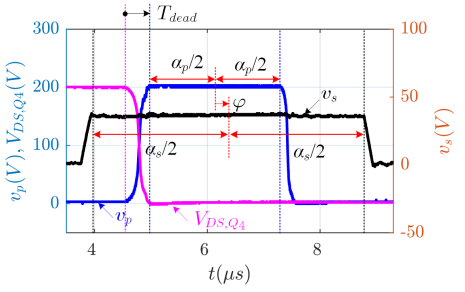


Fig. 3. A detailed description of the three control variables α_p, α_s and φ in practical control.

firstly shown in Section II. Then ZVS analysis concerning the nonlinear change of the output capacitance is conducted in Section III. Next, a comparative analysis with other ZVS calculation methods is presented and verified by experimental results in Section IV, including a comparison with the charge-based method proposed in [10]. At the end, the conclusions are summarized.

II. Practical Switching Transients

A DAB converter topology is shown in Fig. 1. It mainly consists of two full-bridges (i.e. FB_1 and FB_2) generating a two-level or three-level ac voltage (i.e. v_p and v_s) across the transformer-inductor combination. A generalized light-load modulation method [11] is applied and relevant working waveforms are as shown in Fig. 2(a). Therein, three control variables are used to regulate the converter, i.e. duty cycles (α_p, α_s) of v_p, v_s and the phase shift angle (φ) between the

TABLE I
System Parameters of a DAB Prototype

Parameter	Variable	Value
Input DC voltage	V_1	200 V
Output DC voltage	V_2	35 V
Turns ratio of the transformer	$n:1$	3.5 : 1
Switching frequency	f_{sw}	60 kHz
Leakage inductance	L	45 μH

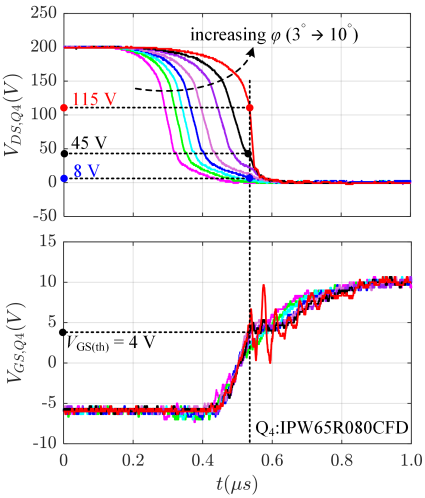


Fig. 4. Measured transient drain-source voltages and gate-source voltages of Q_4 at turning on. Control parameters: $\alpha_p = 60°$, $\alpha_s = 110°$, and $\varphi = 3°, 4°, 5°...10°$ in the 8 cases, respectively.

fundamental components of these two voltages. It is common that a dead time T_{dead} is inserted between the two power devices in the same leg (e.g. Q_2 and Q_4) to avoid short circuit. As a result, this might cause φ to drift in practical control, and hence the dead time effect on the control variables should be considered and properly compensated [12], [13]. In this paper, by using the dead time compensation methods in [12], the practical control variables are depicted in details as shown in Fig. 3.

As highlighted in Fig. 2(a), the power device Q_4 is turned on at $t = t_3$, and meanwhile, Q_2 is turned off and Q_1 is kept on. Consequently, the transient turning on procedure of Q_4 can be described by the FB_1 transition circuit in Fig. 2(b). In a MOSFET device, parasitic capacitances are coupled among the drain, source and gate terminals, denoted by C_{GD}, C_{GS} and C_{DS} in Fig. 2(b). On this basis, a nonlinear characteristic defined by $C_{oss} = C_{GD} + C_{DS}$ is often used to analyze the dynamic switching procedure (cf. Section III).

Using V_1 = 200 V from a dc power source, the measured transient drain-source voltages and gate-source voltages of Q_4 and leakage inductance currents are shown in Fig. 4. The key experimental parameters of the DAB setup are listed in Table I. In Fig. 4, there are 8 groups of $V_{DS,Q4}$ and $V_{GS,Q4}$ corresponding to the phase shift φ varying from 3° to 10°. The

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.3003248, IEEE Transactions on Power Electronics

used power device Q_4 is Infineon IPW65R080CFD, and the threshold voltage $V_{GS(th)}$ = 4 V can be read from the datasheet or manually measured. During the interval $t \in [0.2\ \mu s, 0.6\ \mu s]$, $V_{DS,Q4}$ decreases from V_1 to 0 due to the discharge of output capacitance $C_{oss,Q4}$. In the meantime, $V_{GS,Q4}$ gradually increases and when it reaches $V_{GS(th)}$, the transistor is turned on. Hence, if the drain-source voltage has been reduced to zero or near-zero at this instant, ZVS can be achieved. Otherwise, it transfers to hard switching if $V_{DS,Q4}$ is still relatively high, and $V_{GS,Q4}$ starts to oscillate. In conclusion, in order to realize zero voltage switching of Q_4, the output capacitance $C_{oss,Q4}$ should be sufficiently discharged.

III. Implementation of Nonlinear C_{oss}-V_{DS} Profile in ZVS Analysis

As concluded from the practical switching transients in the last section, the charges stored in the output capacitance should be fully released before turning on in order to achieve ZVS. Hence, in order to obtain an accurate ZVS range, firstly the stored charges should be properly calculated with varying V_{DS} and non-linear C_{oss}. Regarding this, the C_{oss} trajectory hardly varies with the temperature for Si super-junction [14], wide bandgap SiC [15] and GaN [16] devices, and thus the non-linear $C_{oss}-V_{DS}$ profile can be adopted to calculate the stored charges.

As shown in Fig. 2(b), the transient voltages $V_{DS,Q2}$ and $V_{DS,Q4}$ can be described by

$$\begin{cases} C_{oss,Q2}\dfrac{dV_{DS,Q2}}{dt} = -i_{D,Q2} \\ C_{oss,Q4}\dfrac{dV_{DS,Q4}}{dt} = i_{D,Q4} \end{cases} \tag{1}$$

where $i_{D,Q2}$ and $i_{D,Q4}$ are the drain currents of Q_2 and Q_4, respectively. Combining (1) with the following relationship

$$\begin{cases} i_{D,Q4} + i_{D,Q2} = i_p \\ V_{DS,Q4} + V_{DS,Q2} = V_1 \end{cases} \tag{2}$$

leads to

$$i_p = \left[C_{oss,Q2} + C_{oss,Q4}\right]\frac{dV_{DS,Q4}}{dt} \tag{3}$$

For simplification, an equivalent capacitance C_{eq} defined as

$$C_{eq} = C_{oss}(V_1 - V_{DS,Q4}) + C_{oss}(V_{DS,Q4}) \tag{4}$$

is introduced to replace the term $C_{oss,Q2}+C_{oss,Q4}$ in (3). The values of $C_{oss}(V_1 - V_{DS,Q4})$ and $C_{oss}(V_{DS,Q4})$ in (4) can be extracted from the nonlinear $C_{oss}-V_{DS}$ profile shown in Fig. 5(a), which is usually given in the datasheet. Therefore, the C_{eq} trajectory can be obtained as shown in Fig. 5(b).

The equivalent charge Q_{eq} stored in C_{eq} with an off-state drain-source voltage V_1 can be calculated by

$$Q_{eq} = \int_0^{V_1} C_{eq} dV_{DS} \tag{5}$$

The patched area in Fig. 5(b) denotes the charge quantity with V_1 = 200 V.

On the other hand, another condition for ZVS is that the stored charges Q_{eq} can be fully released into the leakage inductance current i_p, which means the conveyed charges in

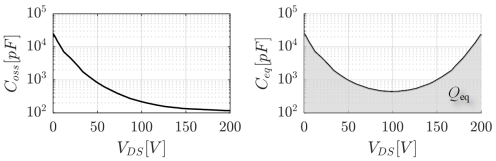


Fig. 5. Nonlinear profiles of (a) C_{oss}, (b) C_{eq} along with V_{DS} for Infineon IPW65R080CFD.

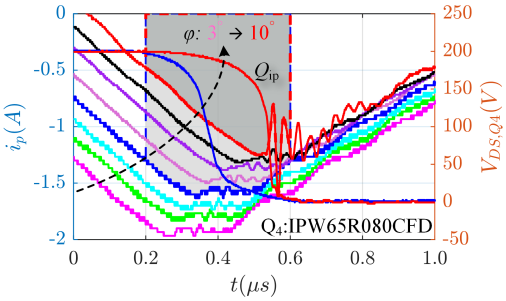


Fig. 6. Measured leakage inductance currents i_p with $\varphi = 3° \sim 10°$ and source-drain voltages $V_{DS,Q4}$ with $\varphi = 6°, 10°$ at the turn-on of Q_4. The lighter and darker patched areas are the conveyed charges Q_{ip} by i_p in the cases of $\varphi = 6°$ and $\varphi = 10°$, respectively.

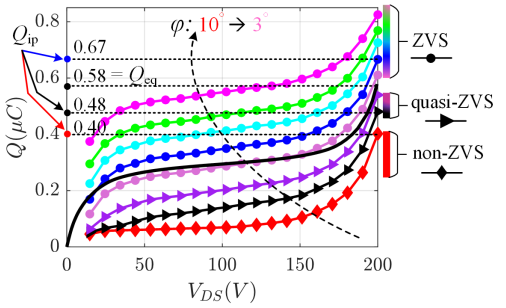


Fig. 7. Numerical integration (i.e. marked lines) of the measured currents i_p and the transient charge of C_{eq} (i.e. solid line) as the drain-source voltage of Q_4 reversely changes from 0 V to 200 V.

i_p should be larger than Q_{eq}. The total charges Q_{ip} in i_p at the turning on of Q_4 could be represented by the patched areas in Fig. 6. Therein, the lighter patched area denotes Q_{ip} in the case of $\varphi = 6°$ and the darker is Q_{ip} in the case of $\varphi = 10°$. It can be seen that the value of Q_{ip} decreases as φ is increased from 3° to 10°. For the convenience of analysis, $t = 0.6\ \mu s$ is deemed the time origin and $t = 0.2\ \mu s$ the transient ending. Therefore, the transient charge Q conveyed by i_p during change of V_{DS} can be calculated by using a numerical integration technique. Corresponding to different φ, the trajectories of Q are shown by different marked lines in Fig. 7. Note that Q is equal to the total charge Q_{ip} when V_{DS} reaches 200 V. As a comparison, the transient charge stored in the equivalent output capacitance C_{eq} is also shown in Fig. 7, denoted by the solid line with a final value of Q_{eq} (cf. Fig.

5(b)).

In the case of $\varphi = 10°$, the available charge $Q_{ip} = 0.4\ \mu C$ in the current is lower than the stored charge $Q_{eq} = 0.58\ \mu C$ in the equivalent capacitance, indicating an insufficient discharge of C_{eq}. Hence, $V_{DS,Q4}$ sharply drops from 115 V to 0 V in less than 0.1 μs (cf. Fig. 4) and severe oscillations are induced in the leakage inductance current. This non-ZVS case should be avoided since it might increase the switching losses and even potentially break the power device [6] due to high dv/dt. In cases of $\varphi = 3°...7°$, the charge Q_{ip} is larger than Q_{eq}, e.g. $Q_{ip} = 0.67\ \mu C$ with $\varphi = 6°$. Therefore, the equivalent capacitance C_{eq} can be totally discharged before Q_4 is turned on. In terms of the middle cases where $\varphi = 8°, 9°$, the transferred charge Q_{ip} (equals 0.48 μC with $\varphi = 9°$) by the current is a bit lower than Q_{eq}, also implying an insufficient discharge of C_{eq}. One difference from the $10°$ case is that the drain-source voltage of Q_4 has reduced to a sufficient low level at turning on, e.g. 45 V for $\varphi = 9°$ and even lower for $\varphi = 8°$ (cf. Fig. 4). Thus no obvious oscillations are stimulated and they are named as quasi-ZVS in Fig. 7. Due to that the switching losses are increased in quasi-ZVS cases (i.e. $\varphi = 8°, 9°$) and the power devices could be impaired in non-ZVS cases (i.e. $\varphi = 10°$), the ZVS is regarded failed in the quasi-ZVS and non-ZVS cases.

IV. ZVS Range Comparison with Experimental Validation

There are mainly three approaches to derive the ZVS range in literature, named as App1, App2 and App3 in the following, and the proposed ZVS range calculation method is represented by Pro..

App1: The most often used method [7] to calculate the ZVS conditions is by

$$I_3 = \frac{nV_2}{4\pi L f_{sw}}\big[(k-1)\alpha_p - 2\varphi\big] \geq 0 \rightarrow \alpha_p \geq \frac{2}{k-1}\varphi \quad (6)$$

where $k = V_1/(nV_2)$ is the input/output dc voltage ratio and f_{sw} is the switching frequency.

App2: Another conventional method [9], [17] to calculate the ZVS conditions is focusing on the energy exchange, leading to

$$\alpha_p \geq \frac{2}{k-1}\varphi + \frac{4\pi L f_{sw}}{(k-1)nV_2}\sqrt{\frac{|\ 4nCV_1V_2 - 2CV_1^2\ |}{L}} \quad (7)$$

where $C = 1/V_1 \int_0^{V_1} C_{oss} dV_{DS}$. In this energy-based method, other than the missing consideration of the non-linearity of the output capacitance, the calculation is complex and it is difficult to achieve the same accuracy as the proposed method. This is because more converter components are involved in the derivation [17], and the calculation will become even more complex if the non-linear C_{oss} is considered.

App3: A third method in [10] is comparing the stored charges Q_{coss} in $C_{oss,Q4}$ (i.e. $Q_{coss} = \int_0^{V_1} C_{oss} dV_{DS}$) with the two defined charges Q_A and Q_B as shown in Fig. 8(a), resulting in

$$\begin{cases} Q_A = -\int_{t_x}^{t_{xy}} i_p dt \geq Q_{coss} \\ Q_B = -\int_{t_{xy}}^{t_y} i_p dt \geq Q_{coss} \end{cases} \Longrightarrow$$
$$\alpha_p \geq max. \left\{ \begin{matrix} \frac{2}{k-1}\varphi + \frac{4\pi f_{sw}}{k-1}\sqrt{\frac{LQ_{eq}}{nV_2}}, \\ \frac{2}{k-1}\varphi + \frac{4\pi f_{sw}}{k-1}\sqrt{\frac{(k-1)LQ_{eq}}{nV_2}} \end{matrix} \right\} \quad (8)$$

Although the non-linearity of the output capacitance is included in this method, the integration limits are not properly considered. As comparison, the integration limits of App3 and the proposed method are depicted in Fig. 8(b), represented by t_x, t_y and t_1, t_2, respectively. It can be seen from Fig. 8(b) that the discharging procedure of the output capacitance of Q_4 is completed within $[t_1,\ t_2]$, which means that this procedure has not began at $t = t_x$ and has finished at $t = t_y$. Therefore, the involved ranges of $[t_x,\ t_1]$ and $[t_2,\ t_y]$ in the calculation (cf. (8)) of the conveyed charges of i_p in App3 is not appropriate. As a result, although the calculated Q_A and Q_B

$$\begin{cases} Q_A = 0.36\ \mu C > Q_{coss} = 0.29\ \mu C \\ Q_B = 0.44\ \mu C > Q_{coss} = 0.29\ \mu C \end{cases} \quad (9)$$

satisfy the ZVS conditions (8) in App3, the soft switching actually fails in the operating case of $\varphi = 10°$ as in shown Fig. 8(a) .

Pro.: Based on the ZVS analysis in Section III, the proposed method of deriving ZVS condition is to compare the stored charges in the equivalent capacitance C_{eq} with the conveyed charges in current i_p during transients, i.e.

$$Q_{ip} = -\int_0^{T_{dead}} i_p dt \geq Q_{eq} = \int_0^{V_1} C_{eq} dV_{DS} \quad (10)$$

The time $0 \rightarrow T_{dead}$ in (10) (cf. Fig. 8(b)) can be mapped to $0.6\ \mu s \rightarrow 0.2\ \mu s$ in Fig. 6. For comparing with App3, the calculated Q_{ip} and Q_{eq} are

$$Q_{ip} = 0.4\ \mu C < Q_{eq} = 0.58\ \mu C \quad (11)$$

and it does not satisfy the ZVS condition (10) of the proposed method, which is consistent with the failed ZVS case in Fig. 8(b).

As discussed in Section III (cf. Fig. 7), the boundary ZVS case is at $\varphi = 7°$. Seen from the practical i_p waveform in the case of $\varphi = 7°$ in Fig. 6, an approximate method to estimate Q_{ip} is by dividing the transient procedure into two intervals

$$i_p = \begin{cases} -I_3,\ t \in \Big[0, \frac{T_{dead}}{2}\Big) \\ -I_3 + \frac{nV_2}{L}\Big(t - \frac{T_{dead}}{2}\Big), t \in \Big[\frac{T_{dead}}{2}, T_{dead}\Big] \end{cases} \quad (12)$$

where $0 \rightarrow T_{dead}/2$ corresponds to $0.6\ \mu s \rightarrow 0.4\ \mu s$ in Fig. 6 and $T_{dead}/2 \rightarrow T_{dead}$ is $0.4\ \mu s \rightarrow 0.2\ \mu s$. In other words, the value of i_p is approximated as constant $-I_3$ in the first half of the dead time and a linear change in the second half. Hence, the ZVS limitation can be further derived by combining (10) and (12), resulting in

$$\alpha_p \geq \frac{2}{k-1}\varphi + \frac{4\pi L f_{sw}}{(k-1)nV_2}\Big[\frac{Q_{eq}}{T_{dead}} + \frac{nV_2}{8L}T_{dead}\Big] \quad (13)$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.3003248, IEEE Transactions on Power Electronics

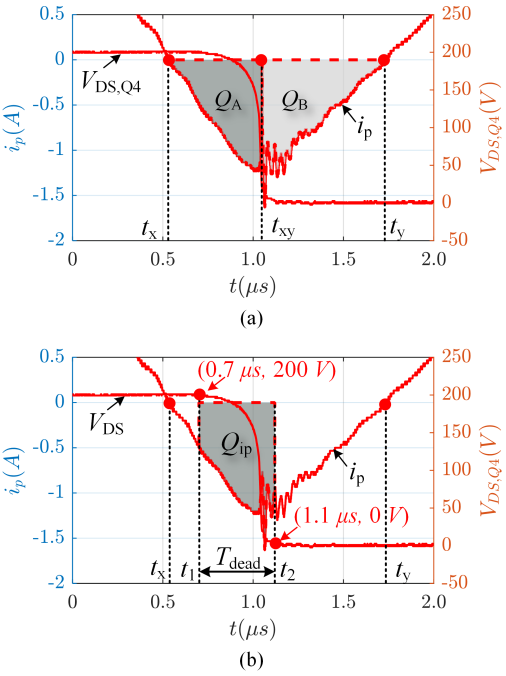


Fig. 8. (a) In the calculation method of App3, the defined two charges Q_A and Q_B in [10] with the case of $\varphi = 10°$, corresponding to the integration ranges of $[t_x,\ t_{xy}]$ and $[t_{xy},\ t_y]$, respectively. (b) In the proposed method Pro., the defined Q_{ip} and relevant integration range $[t_1,\ t_2]$, which is also the dead time interval.

Note that the converter might operate in other working scenarios (e.g. Q_2 turns off before Q_8 turns on in Fig. 2(a)) with a different combination of the three control variables, and in that case, the calculation of the peak value of i_p will be changed accordingly, but the principle of the proposed ZVS range derivation remains the same.

Using the same parameters as in Fig. 4, the calculated ZVS ranges ($\alpha_p - \varphi$ plane) of Q_4 can be obtained with different approaches, as shown in Fig. 9. For practical validation, 24 experimental cases with different system configurations Config.1 $\sim$ Config.3 are also depicted in the figure. The key parameters of the three configurations can be found in Table II. In Config.1, the value of φ is regulated from 3° to 10°, which is the same as Fig. 4, and the boundary is at $\varphi_b = 7°$ (cf. Fig. 7). Note that in order to distinguish the measured experimental ZVS boundary from the calculated results with different methods, φ_b is introduced in Table II to denote the practical ZVS boundary. Similarly, by varying φ between 6° $\sim$ 13° and 9° $\sim$ 16°, the measured ZVS boundaries are found at $\varphi_b = 10°$ and $\varphi_b = 12°$ for Config.2 and Config.3, respectively. As a comparison, the calculated ZVS boundaries using prior-art approaches App1 $\sim$ App3 and the proposed method Pro. are shown in the last four columns of Table II. It can seen that the calculated boundary φ with the proposed

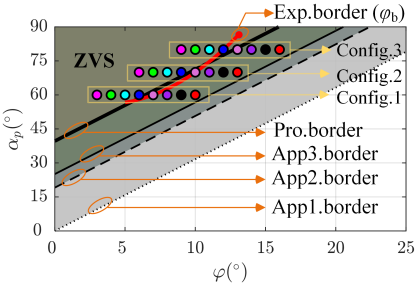


Fig. 9. Calculated ZVS boundaries of Q_4 using prior-art approaches $App1$, $App2$, $App3$ and the proposed method $Pro.$, and experimental cases (denoted by marked points) with different system parameter configurations (cf. Table II) and the obtained experimental ZVS boundaries (i.e. Exp. border).

TABLE II
MEASURED AND CALCULATED ZVS BOUNDARIES FOR DIFFERENT SYSTEM PARAMETER CONFIGURATIONS

Configs.	V_1	V_2	α_p	α_s	$\boldsymbol{\varphi_b}$	App1	App2	App3	Pro.
Config.1	200 V	35 V	60°	110°	**7°**	19°	13°	11°	6.4°
Config.2	200 V	35 V	70°	140°	**10°**	22.2°	16.1°	14.2°	9.6°
Config.3	200 V	35 V	80°	160°	**12°**	25.3°	19.3°	17.4°	12.8°
Config.4	200 V	45 V	110°	160°	**5°**	14.8°	7.3°	6°	5°
Config.5	230 V	25 V	40°	150°	**16°**	32.6°	23.2°	17.6°	15.4°
Config.6	170 V	25 V	40°	150°	**5°**	18.9°	16.4°	8.6°	5.6°

method is more close to the measured φ_b than the other three approaches.

In order to further verify the accuracy of proposed method with different input/output dc voltages, Config.4 $\sim$ Config.6 are implemented. In Config.4, the practical transient waveforms of $V_{DS,Q4}$ and i_p are shown in top inset and middle inset of Fig. 10. Similar to Fig. 7, the numerical integration results are shown in the bottom inset of Fig. 10, from which the measured boundary $\varphi_b = 5°$ can be obtained. Applying the same procedure to Config.5 and Config.6, the measured and calculated ZVS boundaries are as listed in Table II. By comparing the measured boundary φ_b with the calculated values using different methods, the same conclusion can be achieved that the proposed method can predict a more accurate ZVS boundary than the other three methods.

V. CONCLUSIONS

Based on the practical switching transient, an accurate ZVS range calculation method is presented by considering the non-linearity nature of output capacitance in a power device. The method considers both charge and discharge of the power devices in the same bridge leg. On this basis, the concepts of equivalent capacitance and equivalent charge are derived to analyze the ZVS transition and calculate the ZVS range. Compared to prior-art ZVS range calculation approaches where the non-linear output capacitance is not considered, the proposed

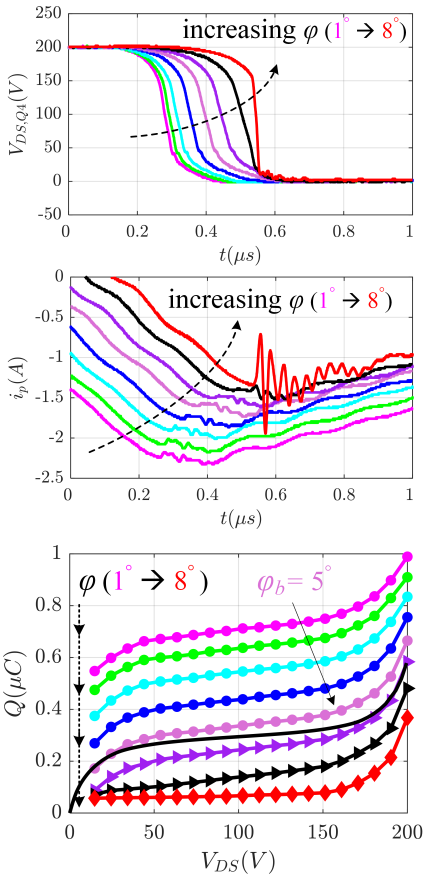


Fig. 10. Measured transients of $V_{DS,Q4}$, i_p and numerical integration of measured i_p for Config.4 in the top inset, middle inset and bottom inset, respectively.

method has a higher accuracy. Although more calculations are needed, this is worthy to use as it is vital in practice to accurately forecast the ZVS boundary. Multiple experiments with different system parameters are implemented and the results are in agreement with the theoretical prediction.

REFERENCES

[1] R. D. Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high power density DC/DC converter for high power applications," in *Conference Record of the 1988 IEEE Industry Applications Society Annual Meeting*, IEEE, 1988.

[2] F. Blaabjerg, Y. Yang, D. Yang, and X. Wang, "Distributed power-generation systems and protection," *Proceedings of the IEEE*, vol. 105, no. 7, pp. 1311–1331, 2017.

[3] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC–DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, Mar. 2012.

[4] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.

[5] H. Chung, S. Y. R. Hui, and K. K. Tse, "Reduction of power converter EMI emission using soft-switching technique," *IEEE Trans. Electromagn. Compat.*, vol. 40, no. 3, pp. 282–287, Aug. 1998.

[6] R. Li, Q. Zhu, and M. Xie, "A new analytical model for predicting dv/dt-induced low-side MOSFET false turn-on in synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5500–5512, Jun. 2019.

[7] G. Oggier, G. O. García, and A. R. Oliva, "Modulation strategy to operate the dual active bridge DC-dc converter under soft switching in the whole operating range," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1228–1236, Apr. 2011.

[8] S. S. Shah, V. M. Iyer, and S. Bhattacharya, "Exact solution of ZVS boundaries and AC-port currents in dual active bridge type DC–dc converters," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5043–5047, Jun. 2019.

[9] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando, and J. Sebastián, "Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 790–804, Feb. 2015.

[10] J. Everts, "Closed-form solution for efficient ZVS modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7561–7576, Oct. 2017.

[11] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[12] D. Segaran, D. G. Holmes, and B. P. McGrath, "Enhanced load step response for a bidirectional DC–dc converter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 371–379, 2013.

[13] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Dead-time effect of the high-frequency isolated bidirectional full-bridge DC–dc converter: Comprehensive theoretical analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1667–1680, 2014.

[14] *Power mosfet electrical characteristics*, TOSHIBA, Jul. 2018.

[15] Z. Chen, D. Boroyevich, R. Burgos, and F. Wang, "Characterization and modeling of 1.2 kv, 20 A SiC mosfets," in *Proc. IEEE Energy Conversion Congress and Exposition*, Sep. 2009, pp. 1480–1487.

[16] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. Rivas-Davila, "Coss losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10 748–10 763, Dec. 2018.

[17] Z. Shen, R. Burgos, D. Boroyevich, and F. Wang, "Soft-switching capability analysis of a dual active bridge dc-dc converter," in *Proc. IEEE Electric Ship Technologies Symp*, Apr. 2009, pp. 334–339.

Conference publication 1

An Optimized Control Scheme for Reducing Conduction and Switching Losses in Dual Active Bridge Converters [C1]

B. Liu, P. Davari and F. Blaabjerg

The paper has been published in
Proc. IEEE ECCE, Sept. 2018, pp. 622-629.

The layout has been revised.

An Optimized Control Scheme for Reducing Conduction and Switching Losses in Dual Active Bridge Converters

Bochen Liu, Pooya Davari, Frede Blaabjerg
Department of Energy Technology
Aalborg University
Aalborg, Denmark
bli@et.aau.dk, pda@et.aau.dk, fbl@et.aau.dk

***Abstract*—An optimized switching control strategy to reduce the conduction and switching losses of the dual active bridge converter is presented in this paper. The control strategy can simultaneously reduce the root mean square value and average absolute value of the leakage inductor current, which are closely relevant to the conduction and switching losses of the semiconductor devices and high-frequency transformers. The optimization is conducted by regulating two manipulated variables on the basis of achieving zero-voltage switching for all switches in a wide voltage range as well as effectively reducing the power losses. An experimental prototype was implemented to validate the theoretical analysis and the feasibility of the proposed method. The experimental results revealed that the converter power losses can effectively be reduced and the overall system efficiency can be improved using the proposed control strategy.**

Keywords—dual active bridge, power losses, zero voltage switching

I. Introduction

The dual active bridge (DAB) converter is now widely used in many applications such as electric vehicles and distributed power systems to adapt different voltage levels and control the power flow among multiple energy sources [1]-[3]. Further advantages, such as having high efficiency, galvanic isolation and bidirectional power flow also make DAB converter as a potential candidate for the future charging systems and vehicle-to-grid (V2G) power transfer.

The DAB converters can operate efficiently when all switches can achieve zero-voltage switching (ZVS), but such efficient operation for the entire power range is only achievable when the voltage ratio is equal to one. If it deviates far from one, the converter efficiency will be greatly reduced in partial loading conditions and even the switches would be broken with excessive *dv/dt* caused by ZVS failure. In order to overcome this drawback, many improved modulation methods are introduced to extend the DAB soft-switching operating range, such as extended phase-shift (EPS) modulation [4], dual phase-shift (DPS) modulation [5], [6] and triple phase-shift (TPS) modulation [7], [8]. In the prior-art phase-shift modulation, the diagonal switches of each full bridge are switched in order to transfer the energy through the linked leakage inductor. Besides, these improved modulation methods generate the driving signals for each switch by adding extra degrees of freedom such that the duty cycle and phase-shift angle of the high-frequency output AC voltage for each full bridge can be also regulated online. Moreover, the converter efficiency and/or power density can be enhanced at the same time if proper optimization methods are applied in [9], but the control complexity is also increased owing to multiple control variables.

In order to further decrease the power degradation of the switches and to reduce the power losses, several hybrid modulation strategies are discussed in [10], [11]. However, the selection and calculation of the optimal modulation parameters are usually complex. On the other hand, minimizing the root mean square (RMS) current of the transformers is introduced in [12], [13] in order to reduce the overall conduction loss and improve the efficiency, but it is often addressed independent from the soft-switching technology for all switches. In fact, the conduction losses of the switches are more related to the average absolute value of the conduction current rather than the RMS value in some specific applications where the insulated gate bipolar transistors (IGBTs) are employed [14] instead of the metal oxide semiconductor field effect transistors (MOSFETs). Besides, as the zero-voltage switching in DAB converters commonly occurs at the instant of turning on, the turn-off switching losses should be also taken into account, especially when higher switching frequency operation is required. Thereby, minimizing the conduction and switching losses are of high importance to both silicon transistors and the new generation power semiconductors like Silicon Carbide (SiC) [15] and Gallium Nitride (GaN) devices [16].

This paper proposes a uniform control scheme to extract the optimal modulation parameters for dual-phase-shift modulation. With the proposed scheme, the conduction and switching losses of the switches and the intermediate transformer are reduced and all switches can achieve soft-switching in a wide voltage range. Firstly, the DAB operation modes are introduced in Section II, and then the conduction and switching losses model are discussed in Section III. Next, the optimized control scheme is explained in Section IV where a comprehensive analysis and comparison among different control schemes is implemented and verified with simulations. In Section V, experimental results are presented to validate the effectiveness of the proposed control scheme. Finally, conclusions are drawn in Section VI.

II. DAB Operation

A DAB converter consisting of two full bridges (HB_1, HB_2) and a high-frequency transformer is shown in Fig. 1. Here, the direction of the power flow is from HB_1 to HB_2 and the converter is assumed to work in voltage boosting mode, namely $V_2>V_1/n$, where n is turns ratio of the isolated transformer. In order to simplify the analysis, all quantities are normalized using the base values as shown in (1) and the voltage ratio k is introduced as V_1/nV_2, which is within (0, 1).

$$P_b = \frac{(nV_1)^2}{8Lf_s} \qquad I_b = \frac{n^2V_1}{8Lf_s} \qquad V_b = V_2 \tag{1}$$

978-1-4799-7312-5/18/$31.00 ©2018 IEEE

P_b, I_b and V_b are the benchmark power, current and voltage, respectively. V_1, V_2 and f_s denotes the input, output dc voltage and the switching frequency, respectively. L is the total inductance referred to the primary side, consisting of the transformer leakage inductor and the auxiliary inductor. The magnetizing inductance of the transformer is considered to be much larger than its leakage inductance. Notably, in order to flexibly adjust the leakage inductance value, an auxiliary inductor is introduced as a part of the equivalent total leakage inductance and it is in series with the primary high-voltage winding to lower the induced additional power losses.

The typical waveforms of the DAB converter with dual-phase-shift (DPS) modulation are illustrated in Fig. 2. The cross switches S_2 and S_3 in the primary full bridge operate synchronously while the switches cascaded in one leg (e.g. S_1 and S_3) operate oppositely and a dead time is introduced in order to avoid short circuit. Thus a 50% duty cycle two-level voltage v_p is generated in the primary full-bridge HB_1. Differently, for the secondary full bridge HB_2, taking the switching signal of S_2 as the reference, the cross switches S_6 and S_7 operate with a shifted angle β_1 and β_2, respectively, resulting in a three-level voltage v_s.

According to whether the falling edge of v_s leads or lags the falling edge of v_p, the DAB converter has two operation modes, namely Mode I as shown in Fig. 2(a) and Mode II as shown in Fig. 2(b). Therein, φ is the phase-shift angle between v_p and v_s, and α represents the duty cycle angle of v_s. The relationship between α, φ and β_1, β_2 can be expressed as:

$$\alpha = \pi - \beta_2 - \beta_1 \qquad \varphi = \frac{\beta_2 - \beta_1}{2} \tag{2}$$

$$\alpha = \pi - \beta_2 - \beta_1 \qquad \varphi = \frac{\beta_2 + \beta_1}{2} \tag{3}$$

(2) and (3) corresponds to Mode I and Mode II, respectively. Therefore, α and φ can be regulated by β_1 and β_2 for both modes. For simplification, D_α and D_φ are defined as:

$$D_\alpha = \frac{\alpha}{\pi} \qquad D_\varphi = \frac{\varphi}{\pi} \tag{4}$$

limited in the range of [0, 1] and [0, 0.5] for D_α and D_φ, respectively. Then the boundary of Mode I and Mode II can be obtained:

$$D_\alpha = 1 - 2D_\varphi \tag{5}$$

which means that if D_α <1-2D_φ, the DAB converter would work in Mode I, otherwise the converter would work in Mode II.

In addition, the secondary current i_s is shaped by the voltage drop on the leakage inductor, that is:

$$\frac{L}{n}\frac{di_s}{dt} = v_p - nv_s \tag{6}$$

So the normalized secondary current based on the switching instant can be derived using (6) following the operating waveforms shown in Fig. 2, as expressed by (7) and (8). In addition, the waveforms of the input and output current (i_1, i_2) of HB_1 and HB_2 are also illustrated in Fig. 2.

$$\text{Mode I} \begin{cases} i_s(t_0) = -\dfrac{2}{nV_1}(k - D_\alpha) \\ i_s(t_2) = \dfrac{2}{nV_1}\left[(1-k)D_\alpha + 2kD_\varphi\right] \\ i_s(t_4) = \dfrac{2}{nV_1}\left[(k-1)D_\alpha + 2kD_\varphi\right] \end{cases} \tag{7}$$

$$\text{Mode II} \begin{cases} i_s(t_0) = \dfrac{2}{nV_1}(1 - k - 2D_\varphi) \\ i_s(t_2) = \dfrac{2}{nV_1}\left[(k+1)D_\alpha + 2kD_\varphi - 2k\right] \\ i_s(t_3) = \dfrac{2}{nV_1}\left[(1-k)D_\alpha + 2kD_\varphi\right] \end{cases} \tag{8}$$

The average output power can be obtained by solving:

$$P_o = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} \left(v_s(t)\cdot i_s(t)\right)dt \tag{9}$$

The normalized results are listed in the third row of Table I and based on those results, Fig. 3(a) depicts the power ranges of Mode I and Mode II, which are segmented by the blue boundary curve. It can be seen that the output power increases with D_α and D_φ in both modes, and the achievable maximum power of Mode II is larger than that of Mode I. Hence, the DAB converter can operate in Mode I for lower power transmission and Mode II for higher output power.

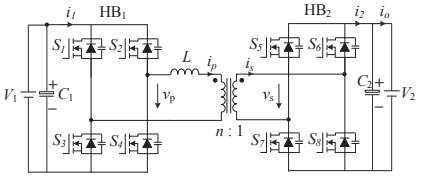
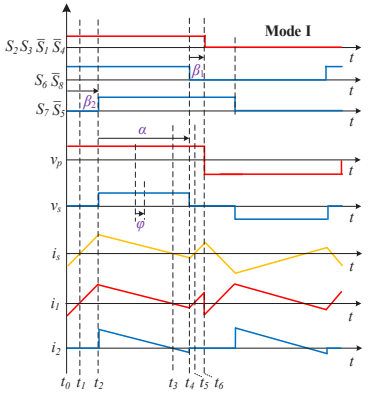
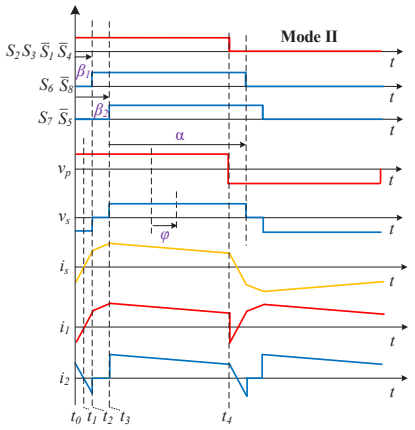


Fig. 1. Dual-active-bridge (DAB) converter topology.

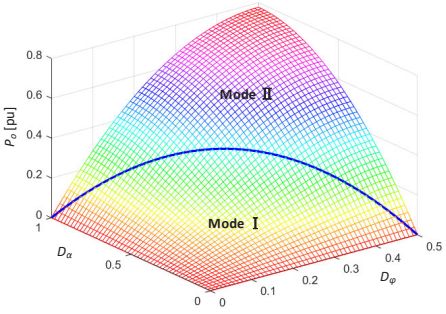


(a)

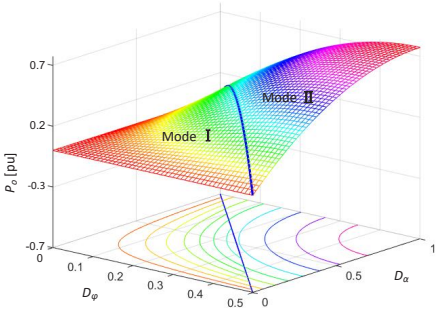


(b)

Fig. 2. Typical waveforms of DAB converters using DPS modulation scheme with k<1 when (a) falling edge of v_s leads v_p (Mode I) (b) falling edge of v_s lags v_p (Mode II)



(a)



(b)

Fig. 3. 3D plot of the power range as the function of D_α and D_φ with the blue curve as the boundary of Mode I and Mode II (a) front view (b) side view with the contour plane of the output power.

III. Losses Analysis and ZVS Conditions

The power losses of the DAB converter include that of the semiconductor devices and transformer. The auxiliary inductor is taken as a part of the transformer because it functions as an equivalent leakage inductance here. Since every switch conducts current for half of the switching period, the power losses of the switches can be calculated by:

$$P_{sw} = \underbrace{\left(\frac{2}{n^2}\frac{R_{DSon,p}}{m_p} + \frac{2R_{DSon,s}}{m_s}\right) I_{s,ms}^2}_{\text{conduction losses}} + \underbrace{\frac{2}{n}\left(t_{on,p} + t_{off,p}\right) V_1 I_{s,dc} f_s + 2\left(t_{on,s} + t_{off,s}\right) V_2 I_{s,dc} f_s}_{\text{switching losses}} \tag{10}$$

where $R_{DSon,p}$, $R_{DSon,s}$ is the on-state resistance of the HB_1, HB_2 transistors, respectively. $I_{s,rms}$ is the root-mean-square value of the secondary transformer current in one switching period:

$$I_{s,\text{rms}} = \frac{1}{T_s}\int_0^{T_s} i_s^2(t)dt \tag{11}$$

Due to the fact that the body diodes of the transistors only conduct during the dead time to achieve ZVS, the conduction losses of the diodes are neglected since the dead time is usually much shorter than the switching period. Note that if paralleled switches are adopted to reduce the conduction losses and increase the supportable current rating, the number of paralleled switches should also be taken into account, represented by m_p and m_s for HB_1 and HB_2, respectively.

On the other hand, the switching losses of the DAB converters can be estimated according to [17], as marked in (10). $t_{on,p}$, $t_{off,p}$ and $t_{on,s}$, $t_{off,s}$ are the turn-on and turn-off time of the switches S_1~S_4 and S_5~S_8, respectively. Here, $I_{s,dc}$ is the average absolute value of the secondary transformer current, which is calculated by:

$$I_{s.dc} = \frac{1}{T_s}\int_0^{T_s} \left|i_s(t)\right| dt \tag{12}$$

For the intermediate high-frequency transformer, the power losses are comprised of two parts: the copper losses of transformer windings and the magnetic core losses. The copper losses can be obtained with:

$$P_{tr,cond} = \left(R_{trs} + \frac{R_{aul} + R_{trp}}{n^2}\right) \cdot I_{s,rms}^2 \tag{13}$$

where R_{aul}, R_{trp} and R_{trs} are the resistances of the auxiliary inductor, primary and secondary winding of the transformer, respectively.

The magnetic core losses are mainly determined by the magnetic flux, the switching frequency, the core volume and the voltage waveform. In order to simplify the core losses calculation, the HF transformer is commonly assumed to be fed with sinusoidal waveforms [18], such that it can be expressed by:

$$P_{tr,core} = k f_s^{\gamma} B^{\sigma} \cdot V_c \tag{14}$$

where k is the material constant, f_s the switching frequency , B the peak flux density and V_c the volume of the magnetic core. γ and σ is the frequency and flux density exponent, respectively, which can be achieved from the core datasheet

TABLE I. EXPRESSIONS AND CONSTRAINTS RELATED TO DAB CONVERTER OPERATION MODES

	Mode I	Mode II
Boundary conditions	$0 < D_\alpha \le 1-2D_\varphi$	$1-2D_\varphi < D_\alpha \le 1$
ZVS constraints	$\frac{2k}{1-k} D_\varphi < D_\alpha < k$	$D_\alpha > 2k\left(1-D_\varphi\right)/\left(1+k\right) \quad D_\varphi > \left(1-k\right)/2$
Normalized output power P_o	$4kD_\alpha D_\varphi$	$-k\left(4D_\varphi^2 - 4D_\varphi + \left(1-D_\alpha\right)^2\right)$
Normalized average absolute secondary current $I_{s.dc}$ [pu]	$\left[\left(-k^2+3k-2\right)D_\alpha^2 + \left(-2k^2+2k\right)D_\alpha + \left(-4D_\varphi^2-1\right)k^2 + k^3\right] / \left(k^2-k\right)$	$\left[\left(-k-1\right)D_\alpha^2 + \left(2k+2\right)D_\alpha + \left(-4D_\varphi^2+8D_\varphi-3\right)k + k^2\right] / \left(1+k\right)$
Normalized RMS value of the secondary current $I_{s.rms}$ [pu]	$\frac{2}{3}\cdot sqrt\left[3\left(k-2\right)D_\alpha^3 + 9D_\alpha^2 + \left(36D_\varphi^2-9\right)kD_\alpha + 3k^2\right]$	$\frac{2}{3}\cdot sqrt\left[-6D_\alpha^3 + \left(-18kD_\varphi+9k+9\right)D_\alpha^2 + \left(36D_\varphi-18\right)kD_\alpha + 3k^2 - \left(6D_\varphi-3\right)\left(2D_\varphi-1\right)^2 k\right]$

and they are commonly considered as constant for a fixed switching frequency.

Comparing (10), (13) and (14), it can be observed that the semiconductor devices power losses and the transformer conduction losses are closely related to $I_{s,rms}$ and $I_{s,dc}$, whereas the transformer core losses are independent on the load current given by (14). This paper will focus on the effect of $I_{s,rms}$ and $I_{s,dc}$ on the converter losses, thus the magnetic core losses are not studied in this paper.

The selected switch types and measured HF transformer parameters for the DAB converter hardware design are listed in Table II. Due to the high current in the low-voltage output side, each switch of HB_2 is composed of two paralleled MOSFETs with a low on-state resistance. The calculated power losses distribution using (10) and (13) are depicted in Fig. 4, from which it can be seen that the transformer resistive losses contributes a large part of the total power losses, highlighting the necessity to reduce the leakage inductance current.

On the other hand, in order to make all switches achieve zero-voltage switching to improve the converter efficiency and avoid voltage spikes induced by hard-switching, the following conditions (15) and (16) should be satisfied in Mode I and Mode II, respectively:

$$i_s\left(t_0\right) < 0 \quad i_s\left(t_2\right) > 0 \quad i_s\left(t_4\right) < 0 \tag{15}$$

$$i_s\left(t_0\right) < 0 \quad i_s\left(t_2\right) > 0 \quad i_s\left(t_3\right) > 0 \tag{16}$$

Together with (7) and (8), the ZVS conditions can be derived as shown in the second row of Table I. the normalized output power P_o and expressions of normalized $I_{s.dc}$ and $I_{s.rms}$ in operation Mode I and Mode II are summarized in Table I.

IV. OPTIMIZED CONTROL SCHEME FOR LOSSES REDUCTION

Seen from Fig. 3(a), there are different combinations of D_α and D_φ to achieve the same output power in Mode I and Mode II, as the contour plane of the output power shown in Fig. 3(b). Therefore, in order to acquire the optimal combination of D_α and D_φ from the power losses reduction point of view, the formulas of $I_{s,dc}$ and $I_{s,rms}$ regarding with D_α and D_φ are deduced using (11) and (12), as listed in Table I. In order to reduce the power losses consumed by the intermediate HF transformer, the values of $I_{s,dc}$ and $I_{s,rms}$ should be decreased according to (10) and (13).

As the colorful surfaces present, Fig. 5 and Fig. 6 illustrate the relationship between $I_{s.dc}$ or $I_{s.rms}$ and D_α, D_φ for respective Mode I and Mode II using the expressions in Table I. In Mode I, there exist a specific point of (D_α, D_φ) for the minimal $I_{s.dc}$ or $I_{s.rms}$. In Mode II, $I_{s.dc}$ is directly proportional to the value of D_α and D_φ, and the behavior of $I_{s.rms}$ is similar to Mode I. Comparing Fig. 5, Fig. 6 and Fig. 3(b), it can be concluded that the conduction and switching losses can be reduced if the proper combination of D_α and D_φ is applied to the converter for different operating power levels.

TABLE II. COMPONENTS OF THE IMPLEMENTED PROTOTYPE

Components	Parameters (@T=25°C)
MOSFETs S_1~S_4: IPW65R080CFD (Infineon)	R_{DSonp} = 72 mΩ
MOSFETs S_5~S_8: 2x IPP110N20N3 (Infineon)	R_{DSons} = 9.6 mΩ
Primary winding of the HF transformer: 35 turns copper foil	R_{trp} = 607.9 mΩ
Secondary winding of the HF transformer: 10 turns copper foil	R_{trs} = 16.5 mΩ
Auxiliary inductor: 10 turns Litz wire, 20 strands, 0.355 mm	R_{aux} = 27.9 mΩ
Magnetic material of the HF transformer	ETD59 ferrite
Magnetic material of the auxiliary inductor	ER42 ferrite

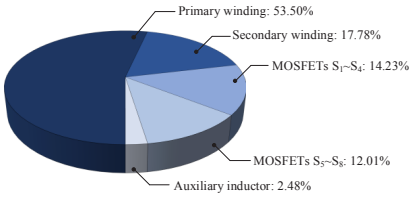


Fig. 4. Caculated losses distribution on the DAB converter components at the output power of 1.5 kW following Table II parameters.

In order to achieve the optimal values of D_α and D_φ for a certain output power, the following equations (17) and (18) can be attained according to the power expressions in Table I, corresponding with Mode I and Mode II.

$$D_\varphi = \frac{P_o}{4kD_\alpha} \tag{17}$$

$$D_\varphi = \frac{k - \sqrt{-k^2 D_\alpha^2 + 2k^2 D_\alpha - kP_o}}{2k} \tag{18}$$

Then by substituting (17) and (18) into the expressions of $I_{s,dc}$ and $I_{s,rms}$, it can be further deduced that when the analytical D_α is equal to the right side of (19) and (20) for Mode I, $I_{s,dc}$ and $I_{s,rms}$ are at their minimum values, respectively.

$$D_{\alpha.dc} = \frac{k\left(1-k+\sqrt{16(1-k)(2-k)D_\varphi^2 + (1-k)^2}\right)}{2(1-k)(2-k)} \tag{19}$$

$$D_{\alpha.rms} = \frac{1-\sqrt{(1-k)^2 - 4k(2-k)D_\varphi^2}}{2-k} \tag{20}$$

Similarly, for operation Mode II, the criteria corresponding to the minimum $I_{s.dc}$ and $I_{s.rms}$ are deduced as (21) and (24), respectively.

$$D_{\alpha.dc} = \frac{2k(1-D_\varphi)}{1+k} \tag{21}$$

Taking into account the ZVS conditions in Table I, the maximum output power for each mode under ZVS can be deduced as:

$$P_{o\max,m1} = 2k^2(1-k) \tag{22}$$

$$P_{o\max,m2} = k \tag{23}$$

where $P_{\text{omax,m1}}$ and $P_{\text{omax.m2}}$ denotes the maximum power of Mode I and Mode II, respectively.

Based on (19), (20), (21), (24), Fig. 7 shows the relationship between D_α and D_φ, where the green curve is for minimized $I_{s.dc}$ and the blue one is for minimized $I_{s.rms}$. Besides, the power curves, the soft-switching area and the boundary of two modes can also be found in the Fig. 7, as displayed by the dashed black curves, the shaded region and the bold line respectively.

The green and blue curves are all within the ZVS area, indicating the minimum $I_{s.dc}$ or $I_{s.rms}$ and ZVS for all DAB switches can be simultaneously achieved. For the power curves, some of them intersect with the green and blue curves in both operation modes, meaning that the power can be reached with minimized $I_{s.dc}$ or $I_{s,rms}$, but it also reveals that the minimization of $I_{s.dc}$ and $I_{s.rms}$ can not be realized at the same time. Furthermore, there are some other power curves separated from minimized $I_{s.dc}$, which can be observed in mode II, implying that the optimal $I_{s.dc}$ can not be reached when the converter works on these power levels. In other words, the switching losses on the semiconductor devices can not be minimized considering (10).

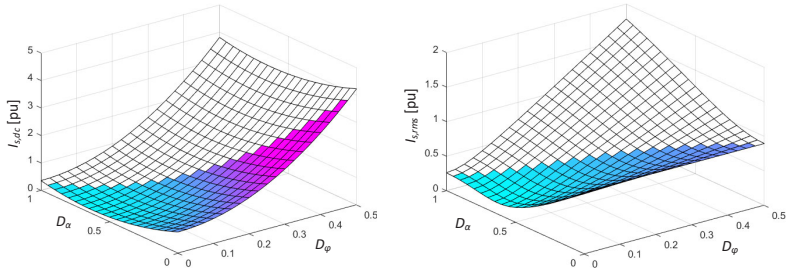


Fig. 5. $I_{s,dc}$ and $I_{s,rms}$ versus D_α and D_φ for operation Mode I: (a) Plane of $I_{s,dc}$ regarding to D_α and D_φ (b) Plane of $I_{s,rms}$ regarding to D_α and D_φ

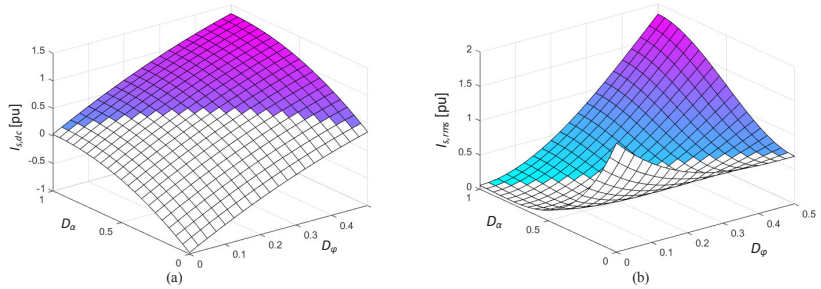


Fig. 6. $I_{s,dc}$ and $I_{s,rms}$ versus D_α and D_φ for operation Mode II: (a) Plane of $I_{s,dc}$ regarding to D_α and D_φ (b) Plane of $I_{s,rms}$ regarding to D_α and D_φ

$$D_{\alpha.rms}=\begin{cases}\dfrac{2D_\varphi+k-1+\sqrt{4\left(k^2+1\right)D_\varphi^2-4\left(k^2-k+1\right)D_\varphi+2k^2-2k+1}}{k}, & \dfrac{1-k}{2}<D_\varphi<\dfrac{k-1+\sqrt{1-k^2}}{2k}\\ 1, & \dfrac{k-1+\sqrt{1-k^2}}{2k}<D_\varphi<0.5\end{cases} \tag{24}$$

Seen from (19), (20), (21), (24), the relationship between D_α and D_φ is segmented and complicated depending on the operation modes and the value of D_φ, which is the root cause of complexity for the minimization of $I_{s.dc}$ or $I_{s.rms}$. In order to simplify the control procedure, a uniform control method is plotted in Fig. 7 using quadratic curve fitting technique, as the red curve presents, which is formulated as:

$$D_{\alpha.opt}=\frac{4(3k-2)}{k(k-2)}D_\varphi^2+\frac{2(2k-1)}{k}D_\varphi+\frac{k}{2-k} \tag{25}$$

Thus the value of D_α and D_φ can be calculated from (25) in both modes, and meanwhile the ZVS conditions are also satisfied as the whole control curve is located in the ZVS area. Besides, it can be seen that all power curves have intersections with the red curve, which indicates a wide power range of the uniform control.

In order to evaluate the effect of the control method on the losses reduction, the simulated total power losses P_{tot} for different output powers are depicted in Fig. 8. The operation state of the DAB converter is determined by the intersection points of the power curve and control curves. Taking Mode I as an example, the DAB converter is controlled by combination (D_α, D_φ) at the operation point B_1, B_2, B_3, B_4 shown in Fig. 7, where no optimization, minimized $I_{s.dc}$ control minimized $I_{s.rms}$ control and the uniform control are employed, respectively. By comparing the simulation results in Fig. 8, the proposed uniform control can effectively reduce the power losses compared to the nonoptimized method and further achieve almost the same power losses as that when the minimized $I_{s.dc}$ or $I_{s.rms}$ is satisfied.

The block diagram of the proposed uniform control scheme for a DAB converter is illustrated in Fig. 9. The operation mode is firstly selected by comparing the given power with the maximum power of each mode, as defined in (22) and (23). Next the actual transmission power P_o is

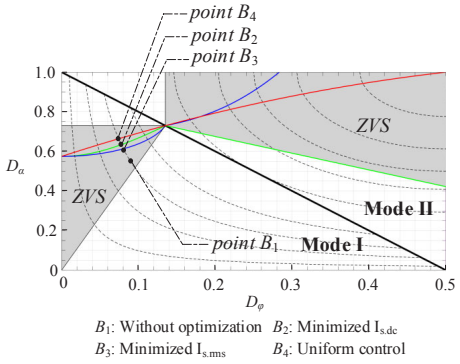


Fig. 7. Curves of different control schemes

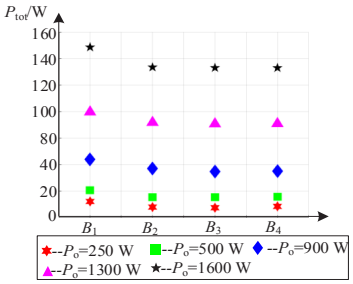


Fig. 8. Simulated total power losses under different control schemes

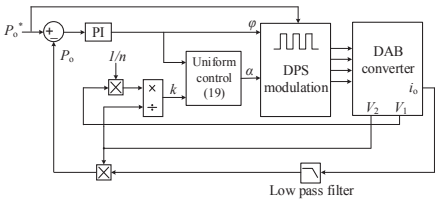


Fig. 9. Block diagram of the proposed uniform control

calculated by multiplying V_2 with the average value of the output current i_o, which can be obtained through a low pass filter. Then the error between the reference value P_o^* and actual P_o is used to produce the phase-shift angle φ between the two full bridges. After the calculation of the voltage ratio k, the other angle α can be achieved using (25). Finally, the two angles are applied to the DPS modulation module and the suitable switching signals are generated.

V. Experimental Verification

An experimental platform for the DAB converter is implemented to validate the proposed uniform control, as shown in Fig. 10. The system parameters are summarized in Table III. The steady state waveforms of the DAB converter in operation Mode I are illustrated in Fig. 11, where v_p and v_s are voltage waveforms generated by HB_1 and HB_2, and i_p, i_s are the primary and secondary transformer current, respectively. Fig. 11(a) shows the measured waveforms when the DAB converter works without adopting any optimal control, which is corresponding to the operation point B_1 in Fig. 7. Fig. 11(b) shows the working waveforms when the converter is modulated by the proposed uniform control, corresponding to the operation point B_4. The output power for both operation points is given at 150 W. As marked in the figure, the value of $I_{s.dc}$ and $I_{s.rms}$ in Fig. 11(b) are both lower than in Fig. 11(a), indicating the effectiveness of the uniform control in reducing the conduction and switching losses of the DAB converter.

TABLE III. PARAMETERS FOR EXPERIMENT

Parameters	Values
High voltage side V_1	190 V
Low voltage side V_2	70 V
Turns ratio of the HF transformer n:1	3.5:1
Switching frequency f_s	60 kHz
Dead time T_{dead}	200 ns
Series inductor L	36.2 μH
Primary side leakage inductance L_{trp}	4.5 μH
Secondary-side leakage inductance L_{trs}	372.5 nH
Primary DC capacitor C_1	0.78 mF
Secondary DC capacitor C_2	1.5 mF

Moreover, Fig. 12 presents the obtained results when the converter works in operation Mode II with a transmission power of 1000 W. The $I_{s.rms}$ in Fig. 12(a) and Fig. 12(b) are 21.95 A and 16.74 A, respectively, and the calculated $I_{s.dc}$ are respective 19.55 A and 14.64 A. Similarly, the lower $I_{s.rms}$ and $I_{s.dc}$ in Fig. 12(b) also validates that the proposed uniform control has a better performance in reducing the converter power losses . Besides, by operating the DAB converter with different transmission power, Fig. 13 plots the measured efficiency curves of the whole system, where blue represents the operation without optimal control and red denotes the uniform control. It can be seen that the system efficiency is improved in the entire power range, especially at light load condition.

In order to evaluate the dynamic response of the proposed uniform control scheme, the DAB converter is controlled to switch between two modes with different given power. The waveforms of the output voltage V_2, the primary voltage v_p, the output current I_o and the output power P_o are measured and displayed in Fig. 14.

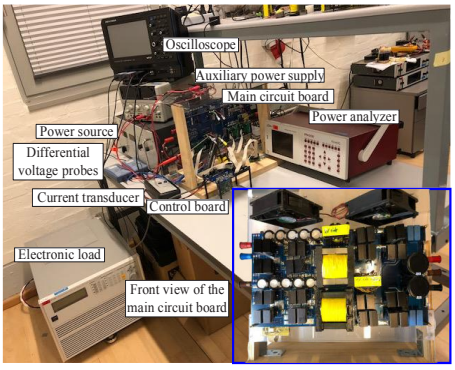
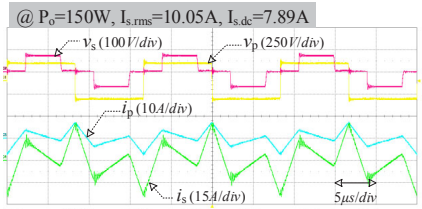
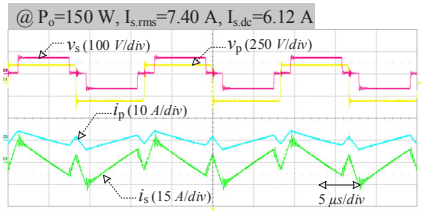


Fig. 10. Test platform for the DAB converter

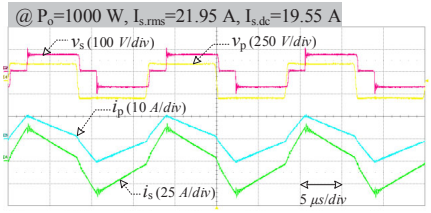


(a)

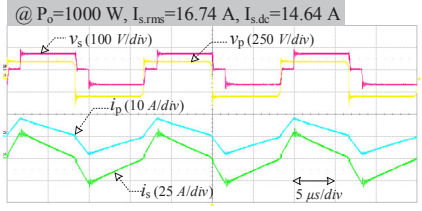


(b)

Fig. 11. Obtained experimental waveforms of DAB converter in operation Mode I: (a) without optimal control (b) with uniform control



(a)



(b)

Fig. 12. Obtained experimental waveforms of DAB converter in operation Mode II: (a) without optimal control (b) with uniform control

The output power is obtained by multiplying the output voltage and output current, which can be realized using the math function of the oscilloscope. The output power is boosted from 460 W to 1120 W at the instant as the blue line shows in Fig. 14(a) and then it is lowered back to 460 W as shown in Fig. 14(b). The DAB converter can automatically switch to the proper operation Mode under the uniform control, which is determined by the given output power. Besides, it can be seen that the DAB converter can reach the new steady state extremely fast after the change of the reference output power.

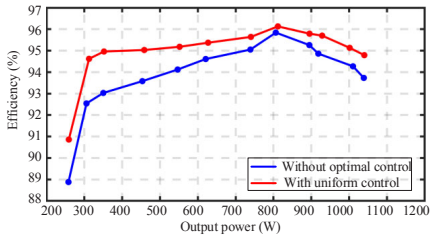


Fig. 13. Measured efficiencies curves of the DAB converter for different output powers

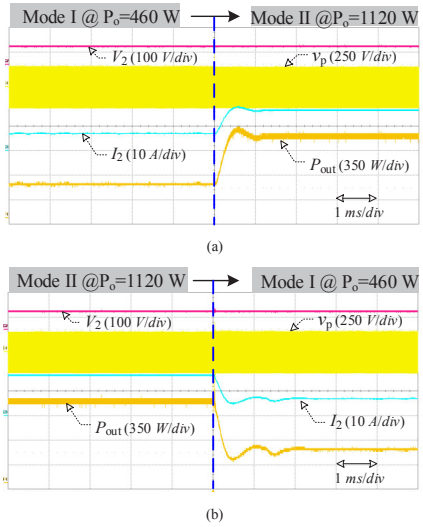


Fig. 14. Dynamic response waveforms of the DAB converter with the output power: (a) inceased from 460W to 1120W (b) decreased from 1120W to 460W

VI. Conclusions

This paper proposes a uniform control scheme to reduce the conduction and switching losses of the DAB converter based on the DPS modulation. Compared to the conventional control methods, the proposed uniform control can not only effectively reduce the switching and conduction losses, which is reflected by the improved converter efficiency, but also lower the control complexity by rearranging the switching signals based on the uniform selection of the control variables in both operation modes. Moreover, the dynamic response of the DAB converter to the change of the output power can be also improved due to the simplified and unified control scheme. Besides, the zero-voltage switching is also guaranteed for all switches in a wide voltage range.

References

[1] G. Ortiz, C. Gammeter, J. W. Kolar, and O. Apeldoorn, "Mixed MOSFET-IGBT bridge for high-efficient medium-frequency dual active-bridge converter in solid state transformers," in *IEEE Workshop on Control and Modeling for. Power Electronics*, 2013, pp. 1–8.

[2] S. Anwar, W. Zhang, F. Wang, and D. J. Costinett, "Integrated dc-dc converter design for electric vehicle powertrains," in *IEEE Applied Power Electronics Conference and Exposition*, 2016, pp. 424–431.

[3] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. D. Doncker, "Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 124–137, Jan. 2015.

[4] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift control of isolated bidirectional dc-dc converter for power distribution in microgrid," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.

[5] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc-dc converters using novel dual-phase-shift control," *IEEE Transactions on Power Electronics*, 2009, pp. 455–452.

[6] F. Li, Y. Li and X. You, "Optimal dual-phase-shift control strategy of an isolated buck–boost converter with a clamped inductor, " *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5374–5385, Jun. 2018.

[7] K. Wu, C. W. De Silva, and W. G. Dunford, "Stability analysis of isolated bidirectional dual active full-bridge DC-DC converter with triple phase shift control," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 2007-2017, Apr. 2012.

[8] A. Taylor, G. Liu, H. Bai, A. Brown, P. Johnson and M .McAmmond, "Multiple-phase-shift control for a dual active bridge to secure zero-voltage switching and enhance light-load performance," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 4584-4588, Jun. 2018.

[9] J. Zhang, J. Lai, R. Kim and W. Yu, " High-power density design of a soft-switching high-power bidirectional dc–dc converter," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1145–1153, Jul. 2007.

[10] J. Everts, J. Van den Keybus, F. Krismer, J. Driesen, and J. W. Kolar, "Switching control strategy for full ZVS soft-switching operation of a dual active bridge AC/DC Converter," in *IEEE Applied Power Electronics Conference and Exposition*, 2012, pp. 1048-1055.

[11] H. Zhou and A. Khambadkone, "Hybrid modulation for dual-active bridge bidirectional converter with extended power range for ultracapacitor application," *IEEE Transactions on Industry Applications*, vol. 45, no. 4, pp. 1434-1442, Jul.-Aug. 2009.

[12] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1215-1227, Apr. 2011.

[13] G. Oggier and M. Ordonez, "High efficiency DAB converter using switching sequences and burst-mode," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2069-2082, Mar. 2016.

[14] P. Davari, Y. Yang, F. Zare and F. Blaabjerg, "A review of electronic inductor technique for power factor correction in three-phase adjustable speed drives," in *IEEE Energy Conversion Congress and Exposition* , 2016, pp. 1-8.

[15] L. Wang, Q. Zhu, W. Yu and A. Huang, "A medium-voltage medium-frequency isolated DC–DC converter based on 15-kV SiC MOSFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 100-109, Mar. 2017.

[16] F. Xue, R. Yu and A. Huang, "A 98.3% efficient GaN isolated bidirectional DC–DC converter for DC microgrid energy storage system applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9094 – 9103, Nov. 2017.

[17] S.Rahman, F. Stückler and K. Siu, "PFC boost converter design guide," Available online at https://www.infineon.com.

[18] W. A. Roshen, "A practical, accurate and very general core loss model for nonsinusoidal waveforms," *IEEE Transactions on Power Electronics*., vol. 22, no. 1, pp. 30–40, Jan. 2007.

Conference publication 2

An Optimized Control Scheme to Reduce the Backflow Power and Peak Current in Dual Active Bridge Converters [C2]

B. Liu, P. Davari and F. Blaabjerg

The paper has been published in the
Proc. IEEE APEC, Mar. 2019, pp. 1622-1628.

The layout has been revised.

An Optimized Control Scheme to Reduce the Backflow Power and Peak Current in Dual Active Bridge Converters

Bochen Liu, Pooya Davari, Frede Blaabjerg
Department of Energy Technology
Aalborg University
Aalborg, Denmark
bli@et.aau.dk, pda@et.aau.dk, fbl@et.aau.dk

***Abstract*—An optimized switching control scheme to reduce the backflow power and the peak current of the dual active bridge converter is presented in this paper. Based on a triple-phase-shift modulation, the control scheme consists of operating the switching devices with three optimized control variables on the basis of achieving a decreased backflow power and peak current. This can enhance the converter efficiency and reduce the current stress on the switching devices. The optimal values of these three manipulated variables are obtained through analysis of different operation modes. Besides, the power transfer ranges and soft-switching constraints are also explained in detail. Experimental results are presented to validate the feasibility of the proposed method.**

Keywords—dual active bridge, backflow power, current stress, triple-phase-shift

I. INTRODUCTION

The bidirectional isolated Dual Active Bridge (DAB) converter is now widely used in many applications such as electric vehicles and distributed power systems to adapt different voltage levels and control the power flow among multiple energy sources [1]-[4]. The advantages of high efficiency, galvanic isolation and bidirectional power flow make it also as a potential candidate for the future charging systems and vehicle-to-grid (V2G) power transfer.

With the everlasting need of higher converter efficiency and power density, over the years many modulation and control strategies have been introduced for DAB converters. For instance, extended phase-shift (EPS) [5], dual phase-shift (DPS) [6]-[8] and triple phase-shift (TPS) [9] modulation methods are proposed to replace the conventional single phase-shift (SPS) modulation, which is simple but having a limited soft-switching range. Therein, the TPS modulation has the highest degree of freedom, and the other modulation methods can be seen as particular cases of the TPS. At the control level, several optimal control strategies can be found in [10]-[12] where reducing the rms value of the leakage inductance current [10], [11] and suppressing the backflow power [12] are commonly used optimization objectives. In most papers, usually one optimization objective is selected to enhance the converter performance. For example, the current stress selected as the optimization target is minimized in [13] whereas the backflow power is considered in [14]. In fact, in terms of TPS modulation, multi-objective optimization is feasible since the TPS has three control variables, which is not addressed in the prior-art research studies.

Different from single-objective optimization, this paper proposes a TPS-based multi-objective optimization control scheme to simultaneously reduce the backflow power and the peak value of the leakage inductance current to improve the system efficiency and reduce the current stress on power semiconductors. By means of analytical calculations, the proposed control scheme can extract the optimal modulation parameters for the DAB converter in a wide voltage range. Firstly, the basic operation modes of the DAB converter are explained in Section II, and then the soft-switching constraints and power transfer range analysis are presented in Section III. Next, the proposed control method to simultaneously reduce the backflow power and the peak leakage inductance current is clarified in Section IV. In Section V, the laboratory prototype and experimental results are illustrated to validate the feasibility of the proposed control scheme. Finally, conclusions are summarized in Section VI.

II. DAB OPERATION MODES

The DAB converter topology is shown in Fig. 1, consisting of two full-bridges on the primary and secondary side of the high-frequency transformer. Usually an auxiliary inductor is put in series with the transformer to serve as part of the equivalent leakage inductance. The intermediate transformer has a turns ratio of n : 1 corresponding to the high-voltage (HV) input and low-voltage (LV) output.

In this paper, the DAB works in voltage boosting mode ($V_1/n < V_2$) and due to the converter symmetry, only positive power transmission is analyzed, namely from the primary high-voltage input to the secondary low-voltage output. In addition, the base value of the power P_b and voltage V_b defined in (1) are used to simplify the calculations. L is the equivalent leakage inductance of the transformer after referring to the primary side and f_{sw} is the switching frequency. The voltage ratio k is introduced as V_1/nV_2, which is within (0, 1).

$$P_b = \left(nV_2\right)^2 \Big/ 8Lf_{sw} \qquad I_b = nV_2 / 8Lf_{sw} \tag{1}$$

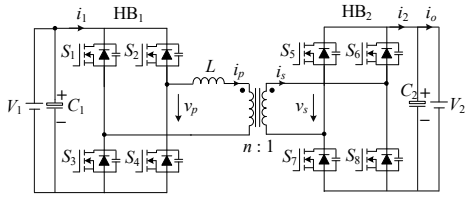
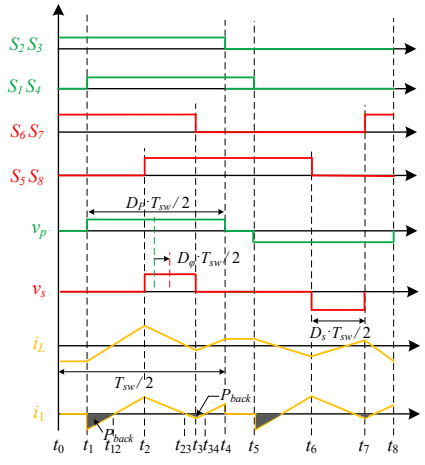


Fig. 1 Dual-active-bridge (DAB) converter topology

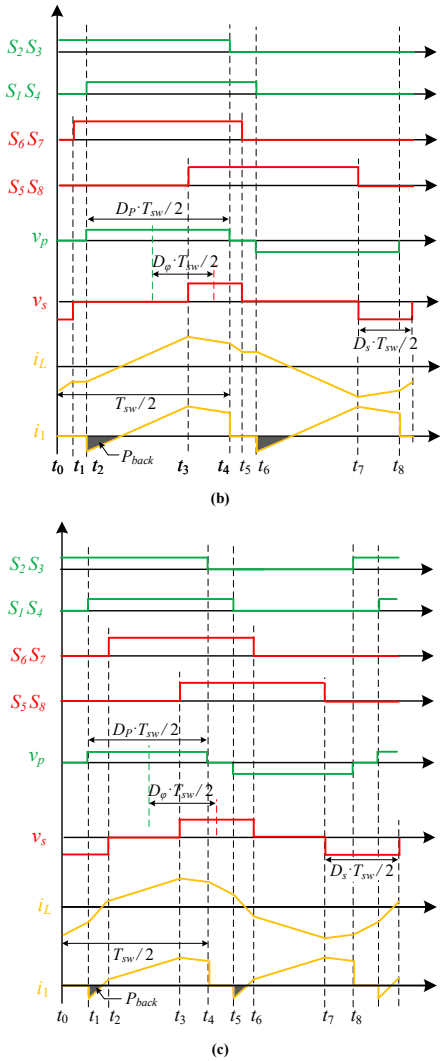
Taking the power transfer direction and voltage boosting into account, the DAB converter can work in four operation modes with TPS modulation [10]. However, as one mode would lead to an increased inductor rms current and does not result in a higher DAB power transfer capability [15], this paper will focus on three operation modes, namely Mode I, Mode II and Mode III as shown in Fig. 2. Therein, D_p, D_s are the duty cycle for the primary voltage v_p and secondary v_s, and D_ϕ denotes the phase-shift angle between v_p and v_s. Each power semiconductor is switched with a 50% duty cycle and the different shifted phases among these switching signals produce numerous values of D_p, D_s and D_ϕ.

Due to the phase-shift operation, only a portion of the power is consumed by the load while the other portion is sent back to the input capacitor C_1, which is called backflow power, as represented by the shaded area in Fig. 2. In order to calculate the average backflow power in half of the switching period, it is necessary to analyze the leakage inductance current first. As shown in Fig. 2(a), the slopes of the leakage inductance current i_L are ruled by the difference between the primary voltage v_p and the secondary voltage v_s, which is expressed in (2).

$$L\frac{di_L(t)}{dt} = v_p(t) - v_s(t) \tag{2}$$



(a)



(b)

(c)

Fig. 2 Operation modes of DAB converters under TPS modulation: (a) Mode I (b) Mode II (c) Mode III

During the four switching intervals in half switching period, i.e. [t_0, t_1], [t_1, t_2], [t_2, t_3], [t_3, t_4], different equations can be derived according to (2), and the zero-crossing instants, i.e. t_{12}, t_{23}, t_{34} also can be obtained in conjunction with the volt-second balance of the leakage inductor. Thus, the average backflow power in half switching period can be calculated as

$$P_{back}=\frac{2V_1}{P_b\cdot T_{sw}}\cdot\left(\int_{t_1}^{t_{12}}\left|i_L(t)\right|dt+\int_{t_{23}}^{t_{34}}\left|i_L(t)\right|dt\right) \tag{3}$$

which is the normalized result considering the reference power P_b.

On the other hand, it can be seen that the peak leakage inductance current appears at the moment of t_2 in Fig. 2(a), and the normalized value is

$$I_{L,peak}=\frac{i_L(t_2)}{I_b} \tag{4}$$

The average backflow power and peak leakage inductance current in the other two modes can also be derived in a similar way based on the working waveforms in Fig. 2(b) and Fig. 2(c).

Besides, in order to appraise the power transfer ability of each operation mode in the following section, the average transmission power in half switching period is needed, which can be obtained by

$$P_o=\frac{2nV_2\cdot\left|\int_{t_r}^{t_f}i_L(t)dt\right|}{T_{sw}\cdot P_b} \tag{5}$$

In (5), t_r and t_f are the point of the rising edge and falling edge of the secondary voltage v_s in half switching period, i.e. [t_r t_f] is [t_2 t_3], [t_3 t_5] and [t_3 t_6] for Mode I, Mode II and Mode III, respectively.

Based on (2)-(5), the derived average transmission power P_o, the backflow power P_{back} and the peak leakage inductance current $I_{L,peak}$ for each operation mode are summarized in Table I with respect to the voltage ratio k and the three control variables D_p, D_s, D_φ.

III. Soft-Switching Constraints and Power Transfer Range

As shown in Fig. 2, the rising and falling edges of the primary voltage v_p and the secondary voltage v_s are interleaved along the time axis. For each operation mode, the relative position relationship of the voltage edges are totally determined by the three control variables D_p, D_s and D_φ. Therefore, the operating modes boundaries also can be depicted with these three variables. Seen from Fig. 2(a) to Fig. 2(c), the phase-shift angle between the primary and secondary voltage is an effective factor provoking the three different operation modes. Therefore, with the shift of D_φ, the DAB converter can work in corresponding mode, as expressed in the second column of Table II. It should be noted that there are some universal limits on the three control variables.

According to the definition in Section II, it can be easily drawn that D_p, D_s have a range of [0, 1] and resulting from the converter symmetry and power direction, D_φ is varied within [0, 0.5]. Besides, in order to ensure that the converter works in voltage boosting situation, $D_p > D_s$ is necessary from the point of realizing soft-switching for all switches in the DAB converter, which will be demonstrated in the following paragraph. $D_p + D_s > 1$ is also predefined so that the converter can transmit relatively higher power.

$$\begin{cases} i_L(t_1)=2\left(D_s-kD_p\right)\le 0\\ i_L(t_2)=4kD_\varphi+\left(2-2k\right)D_s\ge 0\\ i_L(t_3)=4kD_\varphi-\left(2-2k\right)D_s\le 0\\ i_L(t_4)=-2\left(D_s-kD_p\right)\ge 0 \end{cases} \tag{6}$$

$$\begin{cases} i_L(t_1)=2\left(D_s-kD_p\right)\ge 0\\ i_L(t_2)=2\left(D_s-kD_p\right)\le 0\\ i_L(t_3)=4kD_\varphi+\left(2-2k\right)D_s\ge 0\\ i_L(t_4)=4D_\varphi-\left(2-2k\right)D_p\ge 0 \end{cases} \tag{7}$$

$$\begin{cases} i_L(t_1)=4-4D_\varphi-\left(2+2k\right)D_p\le 0\\ i_L(t_2)=\left(2+2k\right)D_s+4k\left(D_\varphi-1\right)\ge 0\\ i_L(t_3)=4kD_\varphi+\left(2-2k\right)D_s\ge 0\\ i_L(t_4)=4D_\varphi-\left(2-2k\right)D_p\ge 0 \end{cases} \tag{8}$$

TABLE I. Output Power, Backflow Power and Inductor Peak Current for Each Opearation Mode

	P_o	P_{back}	$I_{L,peak}$
Mode I	$4kD_sD_\varphi$	$\begin{bmatrix}0.5(1-k)\left(kD_p-D_s\right)^2+0.5(1-k)^2D_s^2\\ -2k(1-k)D_sD_\varphi+2k^2D_\varphi^2\end{bmatrix}\Big/(1-k)$	$2(1-k)D_s+4kD_\varphi$
Mode II	$2k\begin{bmatrix}\left(D_p+D_s-D_\varphi\right)\cdot D_\varphi\\ -0.25\left(D_p-D_s\right)^2\end{bmatrix}$	$\frac{\left(D_s-kD_p\right)^2}{2}$	$2(1-k)D_s+4kD_\varphi$
Mode III	$k\begin{bmatrix}4D_\varphi\left(1-D_\varphi\right)\\ -\left(1-D_s\right)^2-\left(1-D_p\right)^2\end{bmatrix}$	$\frac{k\left[\left(1+k\right)D_p-2\left(1-D_\varphi\right)\right]^2}{2k+2}$	$2(1-k)D_s+4kD_\varphi$

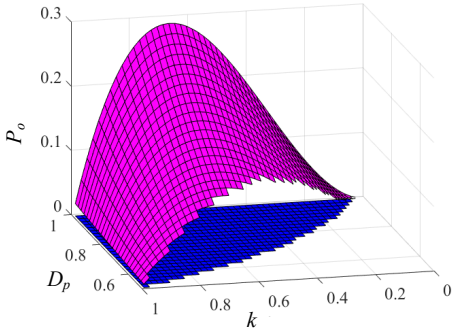
TABLE II. SOFT-SWITCHING CONSTRAINTS AND POWER TRANSFER RANGE FOR EACH OPERATION MODE

	Mode boundaries	Soft-switching constraints	Power transfer range
Mode I	$0 < D_\varphi \le \frac{D_p - D_s}{2}$	$\frac{2k}{1-k} D_\varphi \le D_s \le kD_p$	$0 < P_o \le 2k^2(1-k)\cdot D_p^2$
Mode II	$\frac{D_p - D_s}{2} < D_\varphi \le 1 - \frac{D_p + D_s}{2}$	$D_s = kD_p, \quad D_\varphi \ge \frac{1-k}{2} D_p$	$2k^2(1-k)\cdot D_p^2 < P_o$ $\le (-2k)\cdot\left[\left(k^2+k+1\right)D_p^2 - (2k+2)D_p + 1\right]$
Mode III	$1 - \frac{D_p + D_s}{2} < D_\varphi \le \frac{1}{2}$	$\begin{cases} 0 < D_s \le kD_p, & D_\varphi \ge 1 - \frac{1+k}{2k} D_s \\ kD_p < D_s < 1, & D_\varphi \ge 1 - \frac{1+k}{2} D_p \end{cases}$	$(-2k)\cdot\left[\left(k^2+k+1\right)D_p^2 - (2k+2)D_p + 1\right]$ $< P_o \le k\left(2D_p - D_p^2\right)$

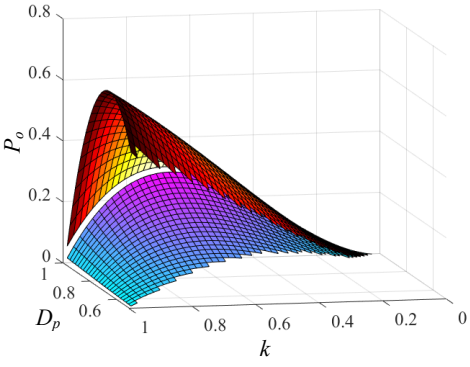
On the other hand, in order to achieve soft-switching for all switches in the converter, the leakage inductance current at the switching instant should follow the rules as expressed in (6), (7) and (8). By solving them, the soft-switching constraints can be obtained for Mode I, Mode II and Mode III, respectively. The results are summarized in the third column of Table II.

Depending on the common limits, the mode boundaries and the soft-switching constraints on the three control variables D_p, D_s and D_φ, the power transfer range of the DAB converter can be developed in different operating modes. Along with the respective transmission power expression in Table I, the minimum and maximum power transfer can be calculated for Mode I, Mode II and Mode III and the results are listed in the last column of Table II.

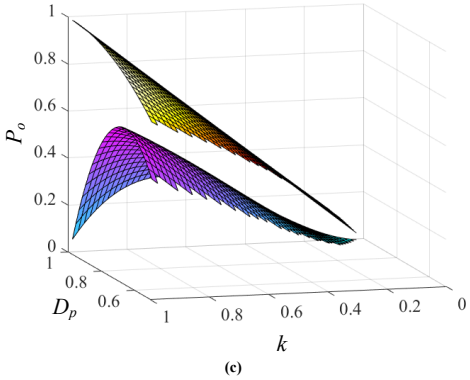
It can be seen that the power transfer range for each mode is dependent on the voltage ratio k and the duty cycle of the primary voltage D_p. Furthermore, based on the calculated results, Fig. 3 illustrates the power transfer range for each operation mode as a function of [k, D_p]. In the three figures, the lower blue surface is the minimum transmission power while the upper red surface represents the maximum power surface. From Fig. 3(a) to Fig. 3(c), it can be concluded that the converter can operate under different output power ranges from light loading up to heavy load conditions.



(a)



(b)



(c)

Fig. 3 Power transfer range for each operation mode with respect to the voltage ratio k and the duty cycle of the primary voltage D_p: (a) Mode I (b) Mode II (c) Mode III. For all the three operation modes, the cool and hot color map denote the minimum and maximum power transfer surfaces, respectively.

IV. Backflow Power and Peak Current Optimization

Seen from the transmission power expressions in Table I, there are infinite combinations of [D_p, D_s, D_φ] for each operation mode to achieve the same power level. Because of this, it is possible to simultaneously reduce the backflow power and the peak inductance current by means of selecting the optimal combination of these three control variables.

Firstly, for the purpose of reducing the average backflow power, taking Mode III as an example, the optimal analytical solution of D_p can be achieved through the partial differential of P_{back}, as expressed by (9).

$$D_p = \frac{2\left(1-D_\varphi\right)}{1+k} \tag{9}$$

It should be noted that the optimization is conducted for a reference output power. See the expression of the average output power in Table I and replace D_p with (9), the expression can be rewritten as

$$P_o = k\left[4D_\varphi\left(1-D_\varphi\right)-\left(1-D_s\right)^2-\left(\frac{1-k-2D_\varphi}{1+k}\right)^2\right] \tag{10}$$

Comparing (10) and the expression of the peak inductance current in Table I, both of them are the function of D_s and D_φ, which means that for a certain output power, there is an optimal combination of [D_s, D_φ] to accomplish the goals of minimizing the peak current and simultaneously satisfying the output power level. In order to find the analytical solution of D_s, the phase-shift angle D_φ is expressed in the explicit function of [D_s, P_o] according to (10), which is

$$D_\varphi = \Big[k^3+k^2+2k- \left(1+k\right)\sqrt{k\left(2k^2+2k-\left(k^2+2k+2\right)\left[k\left(1-D_s\right)^2+P_o\right]\right)}\Big] \Big/ \left[2k\left(k^2+2k+2\right)\right] \tag{11}$$

Then substituting (11) into the expression of $I_{L,peak}$ in Table I, the following (12) can be obtained as the function of D_s.

$$I_{L,peak} = \Big[4+4k+\left(2k^3+2k^2-4\right)\left(1-D_s\right)- 2\left(1+k\right)\sqrt{k\left(2k^2+2k-\left(k^2+2k+2\right)\left[k\left(1-D_s\right)^2+P_o\right]\right)}\Big] \Big/ \left(k^2+2k+2\right) \tag{12}$$

Combining (12) and (10), it can be derived that when D_s is equal to

$$D_s = \frac{\left(2k^3+2k^2-4\right)D_\varphi+2+2k^2}{k\left(k+1\right)^2} \tag{13}$$

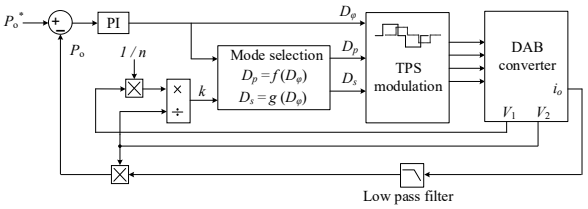


Fig. 4 Block diagram of the proposed optimal control scheme

TABLE III. Relation Expressions of Optimal Control Variables for Each Operation Mode

	Optimal relation expressions	Joint variable limits
Mode I	$D_p = \frac{2D_\varphi}{1-k}$ $D_s = \frac{2kD_\varphi}{1-k}$	$D_\varphi \le \frac{D_p - D_s}{2}$, $\frac{2k}{1-k}D_\varphi \le D_s \le kD_p$
Mode II	$D_p = \frac{2D_\varphi}{1+3k}$ $D_s = \frac{2kD_\varphi}{1+3k}$	$\frac{1-k}{2}D_p \le D_\varphi \le 1-\frac{1+k}{2}D_p$, $D_s = kD_p$
Mode III	$D_p = \frac{2\left(1-D_\varphi\right)}{1+k}$ $D_s = \frac{\left(2k^3+2k^2-4\right)D_\varphi+2+2k^2}{k\left(k+1\right)^2}$	$1-\frac{1+k}{2}D_p < D_\varphi \le 0.5$, $D_s \ge \frac{2k}{1+k}\left(1-D_\varphi\right)$

the minimal peak inductance current is achieved for a reference output power. Therefore, as a function of D_φ and k, (9) and (13) are the optimal D_p and D_s to reduce the backflow power and peak inductance current. In terms of Mode I and II, similar derivation process also can be adopted, and the obtained results are listed in the second column of Table III. Furthermore, the final limits of D_p, D_s and D_φ for each operation mode are also presented in the last column of Table III by joining the mode boundaries and soft-switching constraints in Table II.

The procedure of the proposed control scheme applying to a DAB converter is illustrated in Fig. 4. The actual transmission power P_o is calculated by multiplying V_2 with the average value of the output current i_o, which can be obtained through a low pass filter. Then the error between the reference value P_o^* and actual P_o is used to produce the phase-shift angle D_φ between the two full bridges. At the same time, the operation mode is also selected by comparing the reference power with the three power transfer ranges in Table II.

After the calculation of the voltage ratio k, the values of the other two control variables D_p and D_s can be calculated using the expressions listed in Table III. Together with D_φ, these three control variables are then imported to the TPS modulation module and the switching signals can be generated for the DAB converter accordingly.

V. Experimental Verification

A laboratory prototype shown in Fig. 5 was implemented to verify the effectiveness of the proposed optimized control scheme. The system parameters are listed in Table IV. Taking Mode III as an example, the steady-state operating waveforms of the DAB converter are presented in Fig. 6. v_p and v_s are the voltages generated by the high-voltage side and low-voltage side H-bridge. Since the low-voltage side of the transformer has a larger current than the high-voltage side due to power balance, it will be easier to observe the effect of proposed control scheme on the backflow power reduction. So the waveforms of the secondary current i_s are also shown in Fig. 6.

Fig. 6(a) shows the measured results of the converter under conventional TPS modulation, where the values of the three control variables D_p, D_s and D_φ are selected only based on the reference output power and the soft-switching constraints.

TABLE IV. Parameters for the Experiments

Parameters	Values
High voltage side V_1	100 V
Low voltage side V_2	40 V
Turns ratio of the HF transformer n:1	3.5:1
Switching frequency f_{sw}	60 kHz
Dead time T_{dead}	200 ns
Series inductor L_s	35.9 μH
Leakage inductance of the transformer L_{tr}	17.83 μH

On the other hand, taking the backflow power and peak current reduction into account, Fig. 6(b) shows the measured waveforms of the converter as a result of applying the proposed control scheme into the prototype. The transmission power in these two operating states are both at 400 W. The measured peak value of the inductance current in Fig. 6(a) and Fig. 6(b) is respective 42.35 A and 39.18 A, which validates the effect of the optimized control scheme on reducing the peak current.

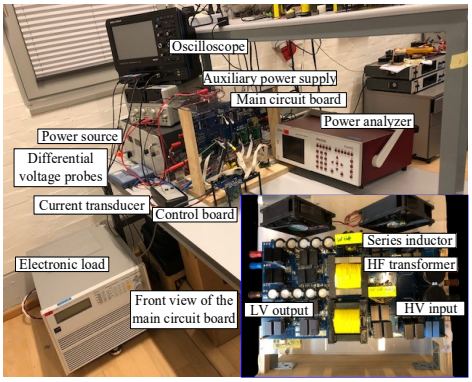
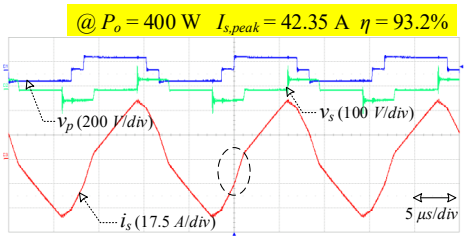
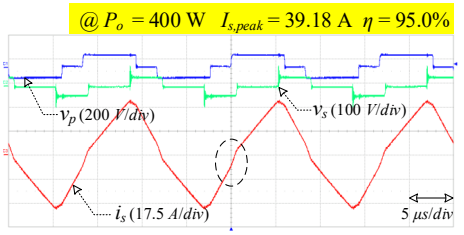


Fig. 5. Test platform for the DAB converter

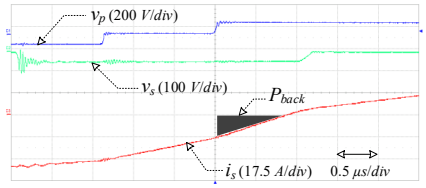


(a)

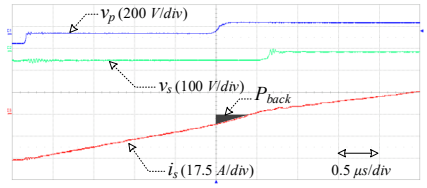


(b)

Fig. 6. Obtained experimental waveforms of DAB converter in Mode III with: (a) conventional control (b) optimized control scheme



(a)



(b)

Fig. 7. Amplified waveforms wrapped by dashed line in Fig. 6(a) and Fig. 6(b), respectively

In order to observe the backflow power, the waveforms wrapped by dashed line in Fig. 6 are amplified by decreasing the time scale, as shown in Fig. 7. It can be seen that the shaded area in Fig. 7(b) is clearly smaller than that in Fig. 7(a), indicating a reduced backflow power in the proposed control scheme. Besides, the system efficiency is also improved from 93.2% to 95.0%, as marked in Fig. 6, which further validates that the proposed optimization scheme can effectively enhance the converter efficiency performance by reducing the backflow power and peak leakage inductance current for the TPS based DAB converter.

VI. Conclusions

This paper proposes an optimized control scheme for DAB converters to reduce the backflow power and peak current based on the TPS modulation. Compared to the conventional method, the proposed control scheme can select the optimal modulation parameters to effectively reduce the backflow power and peak inductance current, thus the system efficiency can be improved and the current stress of the switching devices is decreased. A comprehensive analysis of the soft-switching constraint, power transfer range and optimization process is also explained in detail, which can be further extended to other modulation methods such as DPS and EPS.

References

[1] G. G. Oggier, G. O. García and A. R. Oliva, "Switching Control Strategy to Minimize Dual Active Bridge Converter Losses," in *IEEE Trans. on Power Electronics,* vol. 24, no. 7, pp. 1826 - 1838, 2009.

[2] B. Li, Q. Li, F. C. Lee, Z. Liu and Y. Yang, "A High-Efficiency High-Density Wide-Bandgap Device-Based Bidirectional On-Board Charger," in *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 6, no. 3, pp. 1627 - 1636, 2018.

[3] T. M. Parreiras, A. P. Machado, F. V. Amaral, G. C. Lobato, J. A. S. Brito and B. C. Filho, "Forward Dual-Active-Bridge Solid-State Transformer for a SiC-Based Cascaded Multilevel Converter Cell in Solar Applications," *IEEE Tran. on Industry Applications*, vol. 54, no. 6, pp. 6353 - 6363, 2018.

[4] Z. Wang, B. Liu, L. Guan, Y. Zhang, M. Cheng, B. Zhang and L. Xu, "A Dual-Channel Magnetically Integrated EV Chargers Based on Double-Stator-Winding Permanent-Magnet Synchronous Machines," *IEEE Tran. on Industry Applications*, early access, 2018.

[5] B. Zhao, Q. Yu, and W. Sun, "Extended-phase-shift Control of Isolated Bidirectional DC-DC Converter for Cower Distribution in Microgrid," *IEEE Trans. on Power Electronics*, vol. 27, no. 11, pp. 4667 - 4680, 2012.

[6] H. Bai and C. Mi, "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-active-bridge DC-DC Converters Using Novel Dual-phase-shift Control," *IEEE Trans. on Power Electronics*, vol. 23, no. 6, pp. 2905 - 2914, 2009.

[7] B. Liu, P. Davari and F. Blaabjerg, "An Optimized Control Scheme for Reducing Conduction and Switching Losses in Dual Active Bridge Converters," in *Proc. IEEE Energy Conversion Congress and* Exposition *(ECCE),* 2018, in press.

[8] B. Liu, P. Davari and F. Blaabjerg, "A Flexible Control Scheme for Single-Stage DAB AC/DC Converters," in *Proc. IEEE International Power Electronics and Application Conference and Exposition (PEAC),* 2018, in press.

[9] K. Wu, C. W. De Silva, and W. G. Dunford, "Stability Analysis of Isolated Bidirectional Dual Active Full-bridge DC-DC Converter with Triple Phase Shift Control," *IEEE Trans. on Power Electronics*, vol. 27, no. 4, pp. 2007 - 2017, 2012.

[10] A. K. Jain and R. Ayyanar, "PWM Control of Dual Active Bridge: Comprehensive Analysis and Experimental Verification," *IEEE Trans. on Power Electronics*, vol. 26, no. 4, pp. 1215 - 1227, 2011.

[11] G. G. Oggier and M. Ordonez, "High Efficiency DAB Converter Using Switching Sequences and Burst-mode," *IEEE Trans. on Power Electronics*, vol. 31, no. 3, pp. 2069 - 2082, 2016.

[12] H. Shi, H. Wen, J. Chen, Y. Hu, L. Jiang, G. Chen and J. Ma, "Minimum-Backflow-Power Scheme of DAB-Based Solid-State Transformer With Extended-Phase-Shift Control," *IEEE Trans. on Industry Applications*, vol. 54, no. 4, pp. 3483 - 3496, 2018.

[13] J. Huang, Y. Wang, Z. Li and W. Lei, "Unified Triple-Phase-Shift Control to Minimize Current Stress and Achieve Full Soft-Switching of Isolated Bidirectional DC–DC Converter," *IEEE Trans. on Industrial Electronics*, vol. 63, no. 7, pp. 4169 - 4179, 2016.

[14] F. Xiong, J. Wu, L. Hao and Z. Liu, "Backflow Power Optimization Control for Dual Active Bridge DC-DC Converters," *Energies*, vol. 10, no. 9, 2017.

[15] F. Krismer and J. W. Kolar, "Closed Form Solution for Minimum Conduction Loss Modulation of DAB Converters," *IEEE Trans. on Power Electronics*, vol. 27, no. 1, pp.174 - 188, 2012.

Conference publication 3

Enhanced Zero-Voltage-Switching Conditions of Dual Active Bridge Converter Under Light Load Situations [C3]

B. Liu, P. Davari and F. Blaabjerg

The paper has been published in the
Proc. IEEE APEC, Mar. 2020, DOI: 10.1109/APEC39645.2020.9124213

The layout has been revised.

Enhanced Zero-Voltage-Switching Conditions of Dual Active Bridge Converter Under Light Load Situations

Bochen Liu, Pooya Davari, Frede Blaabjerg
Department of Energy Technology
Aalborg University
Aalborg, Denmark
bli@et.aau.dk, pda@et.aau.dk, fbl@et.aau.dk

***Abstract*— Generally, power electronic converters are designed to obtain the highest efficiency at the rated power while they are partially loaded during most of their operation time. For dual active bridge (DAB) converters, the zero-voltage-switching (ZVS) is prone to failure in light load situations, where precise ZVS conditions are needed but the commonly used current-based and energy-based methods are not good enough to characterize the operating boundaries of the ZVS realization. In this paper, based on the practical turn-on procedure, an improved calculation method of the ZVS condition is introduced here. The method mainly focuses on analyzing the transient procedure during the dead time, by taking into account the non-linearity of the parasitic output capacitance of the transistors. Also, comparative experimental results are shown to validate the feasibility of the analysis.**

***Keywords*—zero voltage switching, dual active bridge, loss estimation**

I. Introduction

One advantage of the DAB converter [1] is the inherent capability of naturally achieving ZVS for all switches without any auxiliary circuits, and this advantage has facilitated a wide application of DAB converters, such as in distributed power systems and energy storage systems [2]–[10]. However, due to the lower leakage inductance current in light-load conditions, the energy stored in the transistor output capacitor may not be totally released during the dead time, and this may result in ZVS failure owing to the high voltage across the transistor at turn-on instant.

There are two commonly used methods to identify the limitations on the control variables for achieving ZVS, i.e. current-based method[11]–[14] and energy-based method [15]. Therein, the current-based method is developed from the body diode conduction when the power device is switched on and thus ZVS conditions can be attained by controlling a positive or negative leakage inductance current at switching instants. In other words, the leakage inductance current are controlled to be larger/smaller than zero at specific switching instants. However, the positive/negative current direction is the result of the ZVS achievement, which is not sufficient in order to guarantee soft-switching. In respect of the energy-based method, the ZVS is achieved under condition that the energy stored in the output capacitance is totally released before the transistor is switched on. Compared to the current-based method, this method is more accurate, which requires a minimum leakage inductance current at the switching instants, not just larger or smaller than zero. However, the non-linearity of the parasitic output capacitance is usually not taken into account, in spite of the fact that the output capacitance of a power device varies a lot during the turn-on/turn-off procedure. Owing to this missed consideration, the obtained ZVS range would contain some critical operating points that could lead to fully ZVS failure.

In this paper, a direct way to derive the zero 'voltage' switching condition is presented by practically analyzing the transient procedure during the dead time. Compared to the current and energy types of ZVS conditions, the proposed voltage-based ZVS conditions have a higher accuracy. Especially, the non-linearity of the parasitic output capacitance (C_{oss}) is also included in the derivation of the ZVS conditions. In the following, the current- and energy-based ZVS derivations are briefly introduced at first, followed by a detailed analysis of the proposed voltage-based method. Furthermore, experimental results are shown to validate the accuracy of obtained ZVS conditions based on the proposed method. In the end, the conclusions are summarized.

II. Conventional ZVS conditions

The DAB topology is shown in Fig. 1(a). Referring to the primary side of the transformer, during different sub-intervals, the leakage inductance current i_p is determined by the voltage drop on the leakage inductance L, which is

$$L \cdot \frac{di_p(t)}{dt} = v_p(t) - nv_s(t) \tag{1}$$

By operating the DAB converter with the generalized triple phase shift (TPS) modulation, the working waveforms of one typical light-load operation mode are as shown in Fig. 2, where D_p and D_s represent the duty cycles of the primary (v_p) and secondary (v_s) voltages of the transformer, respectively, and D_φ is the phase shift ratio between the fundamental components of v_p and v_s. By denoting T_{sw} as the switching period, $D_p \cdot T_{sw}/2$ is the high-level ($+V_1$) time of v_p, which is regulated by the inner phase shift between the transistor Q_1

978-1-7281-4829-8/20/$31.00 ©2020 IEEE

and Q_4 in HB_1. The same meaning is used for $D_s \cdot T_{sw}/2$ in the secondary H-bridge HB_2.

In order to obtain the ZVS conditions for one transistor, the transient turn-on procedure is firstly introduced as follows. In the beginning, the parasitic output capacitance C_{oss} is discharged and the drain-source voltage v_{DS} of the transistor starts to decrease from the turn-off voltage (equal to V_1 for HB_1 transistors and V_2 for HB_2 transistors) to zero. Afterwards, the output capacitance is reversely charged until the voltage v_{Coss} ($v_{Coss} = v_{DS}$) is equal to the forward voltage ($-V_F$) of the anti-parallel body diode. Then the body diode is naturally conducting. During the diode-conducting interval, the drain-source voltage v_{DS} is almost zero and if the transistor is turned on at this moment, ZVS can be achieved. As a consequence, the current is always from the source terminal to the drain terminal when one transistor is softly turned on, and due to this, the direction of the leakage inductance current at switching instants can be confirmed. Together with (1) and the volt-second balance principle, the current-based ZVS imitations on the control variables D_p, D_s and D_φ can be solved. Besides, it can be derived that for the operation mode shown in Fig. 2, the voltage ratio $k = V_1/(nV_2)$ should be larger than 1 to guarantee ZVS for all switches in the converter.

Another type of energy-based ZVS condition is focusing on the energy balance between the transistor output capacitor and the leakage inductor. Through the soft-switching procedure, the key point is to ensure that the resonance between the output capacitors C_{oss} and the leakage inductor L can totally release the energy stored in C_{oss}. On this basis, the relation is $1/2LI_{sw}^2 > h/2C_{oss,eq}V^2$, where I_{sw} is the leakage inductance current at the switching instant, V is the off-state voltage of the transistor and h is the number of charging/discharging transistor output capacitors at the same switching instant. In this method, it requires a minimum value of I_{sw}, not simply larger or smaller than zero as in the current-based ZVS conditions.

Taking the soft turn-on of Q_4 as an example, which happens at the switching instant $t = t_3$ in Fig. 2, the current-based ZVS conditions of Q_4 can be solved as

$$i_p(t_3) = -I_3 = -\frac{nV_2}{4Lf_{sw}}\left[(k-1)D_p - 2D_\varphi\right] < 0 \longrightarrow \quad D_p > \frac{2}{k-1}D_\varphi \tag{2}$$

where I_3 is the absolute value of $i_p(t_3)$, as denoted in Fig. 2. f_{sw} is the switching frequency. At $t = t_3$, Q_1, Q_5, Q_8 are turned on, Q_3, Q_6, Q_7 are turned off, and the output capacitances of Q_2 and Q_4 start resonating with the leakage inductor, as shown in Fig. 1(b). Therefore, combined with (2), the energy-based ZVS conditions of Q_4 can be calculated with

$$\frac{1}{2}LI_3^2 > C_{oss,p}V_1^2 \quad \rightarrow \quad I_3 > V_1\sqrt{\frac{2C_{oss,p}}{L}} \xrightarrow{(2)} \quad D_p > \frac{2}{k-1}D_\varphi + \frac{4kf_{sw}}{k-1}\sqrt{2LC_{oss,p}} \tag{3}$$

by assuming $C_{oss,Q2} = C_{oss,Q4} = C_{oss,p}$.

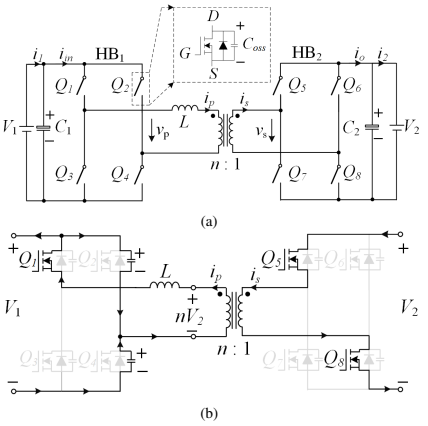


Fig. 1. Operation of the DAB converter (a) DAB topology. (b) Zero-voltage turn-on of Q_4.

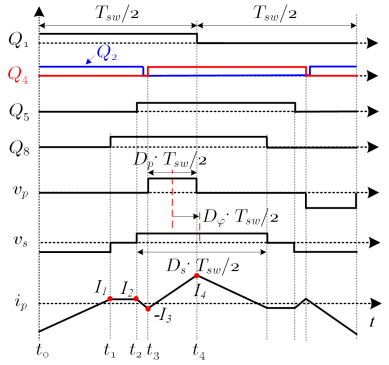


Fig. 2. Typical working waveforms at light load for the DAB converter in Fig. 1(a).

III. Improved ZVS Conditions

As explained in last section, the commonly used types of ZVS conditions are indirectly obtained from the perspective of current direction or energy balance. Both methods are developed based on the ideal switching on/off of the power semiconductor devices, leading to (partly) hard-switching operation within a large portion of the derived ZVS regions. In fact, due to the existence of the parasitic output capacitance, the drain-source voltage v_{DS} across the transistor changes softly from the off-state voltage to zero. This voltage changing process needs time to finish, which is within the generalized dead time in order to avoid short circuit. Furthermore, the non-linearity of the parasitic output capacitance (C_{oss}) is not correctly taken into account in both methods. The values of C_{oss} might change significantly depending on the varying drain-source voltage v_{DS} within the transient procedure. As given in the data sheet, Fig. 3 shows a typical characteristic

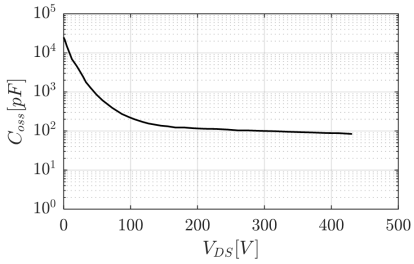


Fig. 3. Non-linear output capacitance $C_{oss}(v_{DS})$ of the used MOSFET IPW65R080CFD.

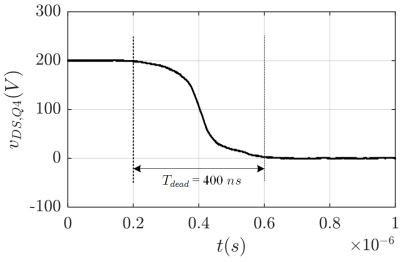


Fig. 4. Measured transient voltage of $v_{DS,Q4}$ during turn-on in a DAB prototype at $V_1 = 200\ V$.

of C_{oss} for the used power device IPW65R080CFD. If v_{DS} varies from 200 V to 0 V during the turn-on procedure, the actual output capacitance increases sharply from 118 pF to the highest 25000 pF, which is a large variation.

In order to further improve the accuracy of ZVS conditions, another type of voltage-based method considering the non-linear parasitic output capacitance is presented in this section.

Seen from Fig. 1(b), the following differential equations can be used to describe the transient voltages of Q_4 and Q_2.

$$\begin{cases} C_{oss,Q2}(v_{DS,Q2})\dfrac{dv_{Coss,Q2}(t)}{dt} = i_{Coss,Q2}(t) \\ C_{oss,Q4}(v_{DS,Q4})\dfrac{dv_{Coss,Q4}(t)}{dt} = i_{Coss,Q4}(t) \end{cases} \tag{4}$$

The items $C_{oss,Qi}(v_{DS,Qi})|_{i=2,4}$ indicates the non-linear output capacitance, and $v_{coss,Qi}$, $i_{Coss,Qi}$ are the voltage and charging/discharging current of $C_{oss,Qi}$. According to Kirchhoff laws, there are

$$\begin{cases} i_p(t) = i_{Coss,Q4}(t) - i_{Coss,Q2}(t) \\ v_{Coss,Q4}(t) = V_1 - v_{Coss,Q4}(t) \end{cases} \tag{5}$$

where V_1 is the off-stage voltage of the power device (equals to the input DC voltage) and $i_p(t)$ is the leakage inductance current, as depicted in Fig. 1(a). Solving (4) and (5) together will lead to

$$i_p(t) = \left[C_{oss,Q2}(v_{DS,Q2}) + C_{oss,Q4}(v_{DS,Q4})\right]\frac{dv_{Coss,Q4}(t)}{dt} \tag{6}$$

Seen from (6), the voltage gradients of $v_{Coss,Q4}$ ($v_{Coss,Q4}$ = $v_{DS,Q4}$) are determined by the current $i_p(t)$ and the summation of the non-linear parasitic capacitance of Q_2 and Q_4. Fig. 4 gives an example of the measured transient drain-source voltages of Q_4 at V_1 = 200 V with a dead time T_{dead} = 400 ns.

In order to simplify the analysis, an equivalent capacitance $C_{eq,Q4}$ is introduced as

$$C_{eq,Q4} = C_{oss,Q4}(v_{DS,Q4}) + C_{oss,Q2}(v_{DS,Q2}) \tag{7}$$

Note that $C_{eq,Q4}$ is also non-linear and changes with the voltage $v_{DS,Q4}$. The used power devices for Q_2 and Q_4 are the same MOSFET IPW65R080CFD, thus the non-linear $C_{oss}(v_{DS})$ curve as shown in Fig. 3 is applicable to both Q_2 and Q_4. Considering the fact that $v_{DS,Q2} + v_{DS,Q4}$ is always equal to V_1, (7) can be transferred into

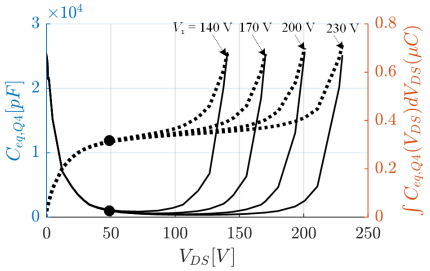


Fig. 5. Profiles of the equivalent capacitance $C_{eq,Q4}$ and charge with different off-state voltages (V_1).

$$C_{eq,Q4} = C_{oss,Q4}(v_{DS,Q4}) + C_{oss,Q4}(V_1 - v_{DS,Q4}) \tag{8}$$

Based on (8), the profiles of $C_{eq,Q4}$ can be described by the solid curves in Fig. 5, which have a "Bathtub-shape". During the turn-on procedure of Q_4, the voltage $v_{DS,Q4}$ decreases softly from the off-stage voltage V_1 to zero. In the meantime, the equivalent output capacitance $C_{eq,Q4}$ firstly decreases sharply and then keeps constant roughly for a while before increasing to the highest value, which aligns well with the changing gradients of the voltage $v_{DS,Q4}$ as shown in Fig. 4.

Moreover, it can be observed from Fig. 5 that the changing trends of $C_{eq,Q4}$ within the range of $V_{DS} \in$ [0 V, 50 V] are the same among different off-state voltages. For addressing this, the integrals of $C_{eq,Q4}$ along the V_{DS} axis are depicted by the dotted curves in Fig. 5. It can be seen that these dotted curves are overlapping in the range of $V_{DS} \in$ [0 V, 50 V]. Therefore, the average value of $C_{eq,Q4}$ within $V_{DS} \in$ [0 V, 50 V] can be used to estimate the drain-source voltage trajectory of Q_4 as $v_{DS,Q4}$ changes from 50 V to 0 V, regardless of the off-stage voltages. For the used MOSFET IPW65R080CFD, the average value is

$$C_{eq,Q4,avg} = \frac{1}{50}\int_0^{50} C_{eq,Q4}(V_{DS})dV_{DS} = 5757\ \text{pF} \tag{9}$$

In order to judge the practical ZVS conditions of Q_4, three experimental cases of ZVS, quasi-ZVS and non-ZVS are shown in Fig. 6. In the three cases, the index "ZVS" indicates ZVS success, "quasi-ZVS" means quasi ZVS success and "non-ZVS" denotes ZVS failure. α_p, α_s, φ equal to $D_p \cdot 180°$, $D_s \cdot 180°$, $D_\varphi \cdot 180°$, respectively, corresponding to the marked control variables in Fig. 2. Actually, the operating points in these three cases are the boundaries of the safe ZVS region, marginal ZVS region and non-VS dangerous region, which will be discussed subsequently.

In the "ZVS" case (blue), as shown in Fig. 6(a), when Q_4 begins to turn on ($v_{\mathrm{GS,ZVS}}$ turns to zero), the drain-source voltage $v_{\mathrm{DS,ZVS}}$ has decreased from the 200 V to 10 V. Then it continuously decreases to zero until $v_{\mathrm{GS,ZVS}}$ rises to the threshold voltage ($v_{\mathrm{GS(th)}}$ = 3.5 V for the used MOSFET IPW65R080CFD). Therefore, the "ZVS" case can achieve the full ZVS operation.

On the other hand, in the "quasi-ZVS" case with larger φ, the drain-source voltage $v_{\mathrm{DS,quasi\text{-}ZVS}}$ is as high as 70 V when the driving signal $v_{\mathrm{GS,quasi\text{-}ZVS}}$ becomes positive. But then it rapidly decreases to around 15 V by the time $v_{\mathrm{DS,quasi\text{-}ZVS}}$ reaching the threshold voltage. Thus this case is termed as quasi-ZVS operation.

By keeping the same α_p and α_s, the value of φ is adjusted to higher 10° in the "non-ZVS" case. As seen from Fig. 6(b) and Fig. 6(d), the gate-source voltage and the leakage inductance current start to oscillate due to the ZVS failure. This voltage and current oscillations might damage the power devices and the gate driver, and hence the related operating points are named as dangerous region.

Comparing the transient waveforms of $v_{DS}(t)$ in Fig. 6(a), it can be found that $v_{DS,Q4}$ has a sharp plunge from the off-state voltage to zero in the ZVS failure case. In contrast, $v_{DS,Q4}(t)$ softly decreases to zero in the other two cases. Based on (6) and (7), the voltage shape of $v_{DS,Q4}$ (equals to $v_{Coss,Q4}$) is affected by the non-linear $C_{eq,Q4}$ and the leakage inductance current $i_p(t)$. But due to the variations of $C_{eq,Q4}$ and $i_p(t)$, it is difficult to directly solve the transient voltage $v_{DS,Q4}$. Thus (6) is transformed into the following integral form

$$\int_0^{v_{DS,ins}} C_{eq,Q4}(v_{DS,Q4})dv_{DS,Q4} = \int_0^{t_{ins}} i_p(t)dt \quad (10)$$

where $v_{DS,ins}$ is the instantaneous drain-source voltage at any time instant $t = t_{ins}$ during the transient procedure. It can be seen that both sides of (10) mean the concept of charge Q. In order to fully charge/discharge the parasitic output capacitance $C_{oss,Q2}$ and $C_{oss,Q4}$, the right side of (10) should be larger than the left side. Otherwise, one of the two situations of quazi-ZVS or non-ZVS would happen, depending on the remaining time from $v_{DS,Q4}$ = 50 V to $v_{DS,Q4}$ = 0 V, which will be explained later.

Using the extracted waveform data of $v_{DS,Q4}(t)$ and $i_p(t)$, the integrals of the leakage inductance currents in eight experimental cases are shown in Fig. 7. To align with the integrals in (10) where the initial $v_{DS,Q4}$ is zero, the time sequence is reversed from the end to start of the dead time interval. Besides, the signs of the $i_p(t)$ integrals are also reversed to positive so as to compare with the integrals of

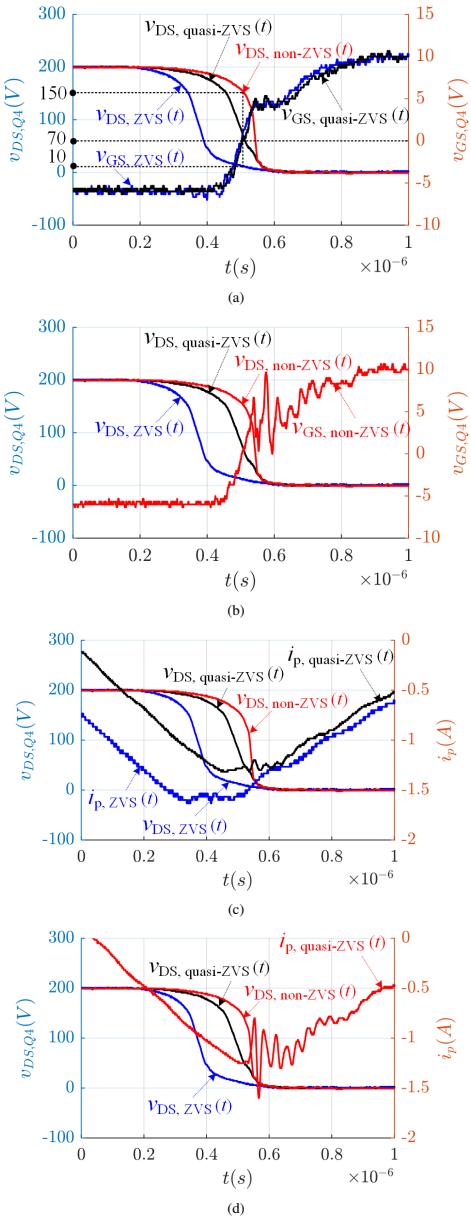


Fig. 6. Three experimental cases of the ZVS operation, quasi ZVS operation and ZVS failure of Q_4. blue: ZVS success (safe region), $\alpha_p = 60°$, $\alpha_s = 110°$, $\varphi = 6°$. black: quasi ZVS (marginal region), $\alpha_p = 60°$, $\alpha_s = 110°$, $\varphi = 9°$. red: ZVS failure (dangerous region), $\alpha_p = 60°$, $\alpha_s = 110°$, $\varphi = 10°$.

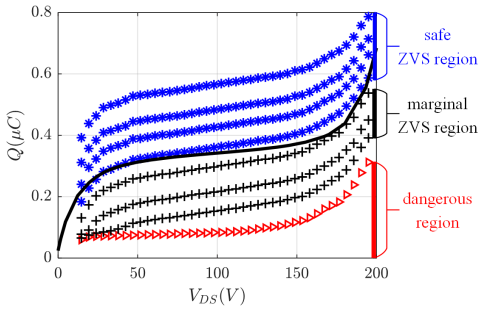


Fig. 7. The calculated integrals of $i_p(t)$ in eight experimental cases. blue "*": Case 1 to Case 4 from top to bottom (safe ZVS region). black "+": Case 5 to Case 7 from top to bottom (marginal ZVS region). red "▷": Case 8 (dangerous region). $\alpha_p = 60°$, $\alpha_s = 110°$ are applied to the eight cases, and $\varphi = 3°, 4°...10°$ in Case 1, 2..8, respectively. Therein, Case 4, Case 7 and Case 8 correspond to the "ZVS" case, the "quasi-ZVS" and the "non-ZVS" case in Fig. 6. Besides, the integral of $C_{eq,Q4}$ over various v_{DS} is depicted by the solid curve.

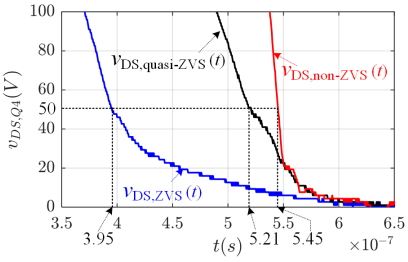


Fig. 8. Zoomed waveforms of $v_{DS,Q4}$ of the three cases in Fig. 6.

$C_{eq,Q4}$ in Fig. 7. According to the previous discussion, the Q-V_{DS} plane is divided into three regions: safe ZVS region (where ZVS is totally achieved), marginal ZVS region (where ZVS is quasi achieved without damaging the power devices or gate drivers) and dangerous region (where ZVS totally fails). As the phase shift φ increases from 3° to 10° in the eight cases, the operating points location gradually changes from the safe region to the dangerous region.

In order to judge the boundary conditions among the three regions, the waveforms of $v_{DS,Q4}$ are zoomed in Fig. 8. At the time instants $t = 0.395\ \mu s$ and $t = 0.521\ \mu s$, the drain-source voltages of the "ZVS" and "quasi-ZVS" cases (blue and black) are both equal to 50 V, so that there is enough time left for Q_4 to release the stored energy in the output capacitance. Whereas in the "non-ZVS" case (red), the $v_{DS,Q4}$ keeps a much higher voltage than 50 V until $t = 0.545\ \mu s$, resulting in little time left to totally discharge the output capacitance before the end of the dead time and thus leading to ZVS failure. Apart from the non-linear parasitic output capacitance, the transient drain-source voltage is also slightly influenced by the leakage inductance current. As it can be seen in Fig. 6(c), the current $i_p(t)$ is almost constant during $v_{DS,Q4} \in$ [0 V, 50 V], and it equals to $-I_3$, which is marked in Fig. 2. Similar as before, by setting $t = 0.611\ \mu s$ (when all $v_{DS,Q4}$ decrease to zero) in Fig. 8 as the origin $t = 0$, the original $t = 0.395\ \mu s$ is transformed into $\Delta t = 0.216\ \mu s$. The ZVS boundary conditions of the safe ZVS region and the marginal ZVS region can be derived by satisfying

$$\int_0^{\Delta t} I_{3,min} dt \geq \int_0^{50} C_{eq,Q4,avg} dv_{DS,Q4} \tag{11}$$

Equation (11) implies that in order to achieve total ZVS for Q_4, the parasitic output capacitance $C_{oss,Q2}$ and $C_{oss,Q4}$ should not only totally charge/discharge, but also be completed within a limited time interval.

Due to the fact that the operating points in marginal ZVS region do not need to fulfill (11), the minimum I_3 can only be obtained from the boundary "quasi-ZVS" case (i.e. the "quasi-ZVS" case in Fig. 6 or Case 7 in Fig. 7). Similarly, to simplify the calculations, the original $t = 0.611\ \mu s$ in Fig. 8 is set as the origin $t = 0$, then the original $t = 0.521\ \mu s$ is transformed into $\Delta t_m = 0.09\ \mu s$. As a result, the following equation should be met.

$$\int_0^{\Delta t_m} I_{3,min} dt \geq -\int_0^{\Delta t_m} i_p(t) dt \tag{12}$$

Using the calculated $I_{3,min}$ by (11) or (12), the ZVS limitations on the control variables can be derived by

$$\begin{aligned} I_3 = \frac{nV_2}{4Lf_{sw}}\left[(k-1)D_p - 2D_\varphi\right] \geq I_{3,min} \\ \longrightarrow D_p > \frac{2}{k-1}D_\varphi + \frac{4Lf_{sw}}{nV_2(k-1)}I_{3,min} \end{aligned} \tag{13}$$

The same procedure can be applied to the other switching instants (e.g. t_1, t_2, t_4) in a half switching period and the calculated ZVS limitations are summarized in the last column of Table I. $I_{1,min}$, $I_{2,min}$ and $I_{4,min}$ are the minimum leakage inductance currents needed to achieve total ZVS or marginal ZVS of Q_8, Q_5, Q_3, respectively. Due to the mirror symmetry of the working waveforms in one switching period, the two power devices in one leg share the same ZVS conditions. Hence the ZVS conditions for Q_8, Q_5, Q_4, Q_3 are also applicable to Q_6, Q_7, Q_2, Q_1, respectively.

Besides, similar to (2) and (3), the derived voltage-based and energy-based ZVS limitations at different switching instants are also listed in Table I. For a clear comparison, an example of the ZVS range is calculated by the three methods and it is shown in Fig. 9.

Seen from the top inset in Fig. 9, owing to the ignorance of the transient turn-on procedure in current-based method, a large portion of the induced ZVS range (wrapped by solid lines) is the dangerous region. The same issue exists in the energy-based ZVS region (wrapped by dashed lines) due to the disregard of the non-linearity of the parasitic output capacitance. In the voltage-based method, the three regions discussed above are depicted in Fig. 9 and partly amplified for a clear view in the bottom inset. These three regions are identified by the safe ZVS conditions (11) and the quasi-ZVS conditions (12). Detailed information can be found in the caption note of Fig. 9

TABLE I
THREE TYPES OF ZVS LIMITATIONS ON THE CONTROL VARIABLES FOR DAB CONVERTERS

t (ref. Fig. 2)	Current-based	Energy-based	Voltage-based (proposed)
t_1, Q_8	$D_s > kD_p$	$D_s > kD_p + \frac{4}{n} f_{sw}\sqrt{2LC_{oss,s}}$	$D_s > kD_p + \frac{4Lf_{sw}}{nV_2} I_{1,min}$
t_2, Q_5	$D_s > kD_p$	$D_s > kD_p + \frac{4}{n} f_{sw}\sqrt{2LC_{oss,s}}$	$D_s > kD_p + \frac{4Lf_{sw}}{nV_2} I_{2,min}$
t_3, Q_4	$D_p > \frac{2}{k-1} D_\varphi$	$D_p > \frac{2}{k-1} D_\varphi + \frac{4kf_{sw}}{k-1}\sqrt{2LC_{oss,p}}$	$D_p > \frac{2}{k-1} D_\varphi + \frac{4Lf_{sw}}{nV_2(k-1)} I_{3,min}$
t_4, Q_3	$D_p > -\frac{2}{k-1} D_\varphi$	$D_p > -\frac{2}{k-1} D_\varphi + \frac{4kf_{sw}}{k-1}\sqrt{2LC_{oss,p}}$	$D_p > -\frac{2}{k-1} D_\varphi + \frac{4Lf_{sw}}{nV_2(k-1)} I_{4,min}$

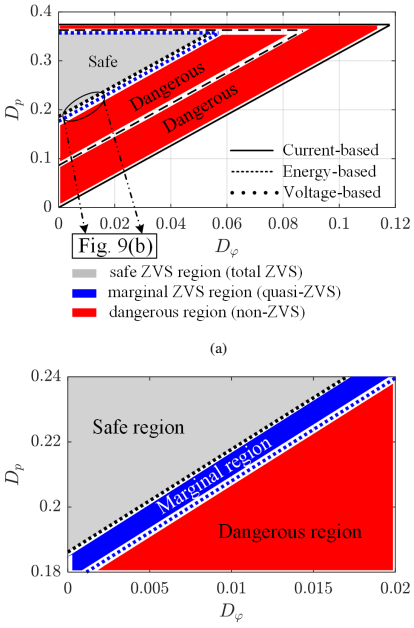


Fig. 9. (a) ZVS range comparison among the current-based, energy-based and voltage-based methods. (b) Zoomed view of Fig. 9(a). In the voltage-based method, the three regions discussed before are depicted, i.e. safe ZVS region (total ZVS achieves), marginal ZVS region (quasi-ZVS achieves), and dangerous region (ZVS fails). Following parameters are used: $D_s = 0.61$, $k = 1.63$ are applied in current-based method. $L = 45\ \mu H$, $n = 3.5$, $f_{sw} = 60\ kHz$, $C_{oss,p} = 215\ pF$, $C_{oss,s} = 401 \times 2\ pF$ are used in energy-based method. $V_2 = 35\ V$, $I_{1,min} = I_{2,min} = 1.5\ A$ are adopted in voltage-based method. Notably, in the energy-based method, $C_{oss,p}$ is the typical output capacitance of IPW65R080CFD, and $C_{oss,s}$ is double times the typical value of IPP110N20N3G because two MOSFETs are paralleled for each switch in HB_2. In the voltage-based method, $I_{3,min} = 1.34\ A$ (obtained from (11)) is used to specify the safe region boundary and $I_{3,min} = 0.32\ A$ (obtained from (12)) the marginal ZVS region boundary.

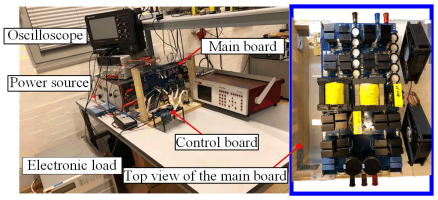


Fig. 10. Test platform for the DAB converter.

TABLE II
SYSTEM SPECIFICATIONS FOR DAB CONVERTER

Parameters	Description	Value
P	Rated power	1.5 kW
V_1	Input DC voltage	230 V
V_2	Output DC voltage	25 V
$n:1$	Turns ratio of the transformer	3.5 : 1
f_{sw}	Switching frequency	60 kHz
T_{dead}	Dead time	400 ns
L_s	Series inductor	36.2 μH
L_{trp}	Primary-side leakage inductance	4.5 μH
L_{trs}	Secondary-side leakage inductance	372.5 nH
C_1	Primary DC capacitor	0.78 mF
C_2	Secondary DC capacitor	1.5 mF

IV. EXPERIMENTAL VALIDATION

A test platform shown in Fig. 10 is built and the converter parameters are listed in Table II. The used transistor type is IPW65R080CFD in HB_1 and two IPP110N20N3 are in parallel for each switch in HB_2. In order to validate the universality of the proposed method, the DAB setup is operated with another group of input (V_1) and output (V_2) DC voltages, as listed in Table II.

Using the new group of V_1 and V_2 (different from $V_1 = 200\ V$, $V_2 = 35\ V$ in Fig. 9), the enhanced ZVS range can be calculated by the proposed voltage-based method, and a similar D_p-D_φ plane including different ZVS regions and dangerous region is as shown in Fig. 11. Due to the changed voltage ratio $k = V_1/(nV_2) = 2.63$ and the secondary duty ratio $D_s = 0.833$, the ZVS ranges in Fig. 11 are different from Fig. 9 (where $k = 1.63$, $D_s = 0.61$) with a wider range of D_φ and a narrower range of D_p. In order to verify the effectiveness of the obtained ZVS regions in Fig. 11,

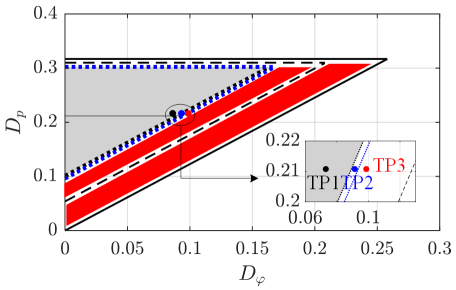


Fig. 11. ZVS limitations derived from the proposed method by setting different input and output DC voltages (V_1 = 230 V, V_2 = 25 V) and selecting three test points for the experimental validation. The meanings of the curve types and shaded areas are the same as Fig. 9. Test point 1 (TP1): safe ZVS region, D_p = 0.212, D_s = 0.833, D_φ = 0.067. Test point 2 (TP2): marginal ZVS region, D_p = 0.212, D_s = 0.833, D_φ = 0.094.. Test point 3 (TP3): dangerous region, D_p = 0.212, D_s = 0.833, D_φ = 0.1.

three test points from the safe ZVS region, the marginal ZVS region and the dangerous region are applied to the DAB prototype, as indicted by "TP1", "TP2" and "TP3" in the amplified inset. The matching operating waveforms are shown in Fig. 12(a), Fig. 13(a) and Fig. 14(a), respectively. v_p and v_s are the primary and secondary terminal voltages of the two H-bridges HB_1 and HB_2, respectively. i_p is the leakage inductance current, which is also the output terminal current of the primary HB_1 and thus denoted with the item "p".

In order for a clear view of the transient turn-on procedure, the shaded gray areas in Fig. 12(a) to Fig. 14(a) are zoomed in Fig. 12(b) to Fig. 14(b), respectively. As the converter operates from TP1 (total ZVS) to TP3 (ZVS failure), the gradients of the drain-source voltage $v_{DS,Q4}$ gradually changes more and more sharply, and eventually results in a large $v_{DS,Q4}$ when the gate-source voltage $v_{GS,Q4}$ reaches the threshold voltage (= 3.5 V) in Fig. 14(b). This would lead to voltage spikes of v_p (as highlighted by the black ellipse in Fig. 14(a)), while the waveforms of v_p in Fig. 12(a) and Fig. 13(a) are clear and soft at the same switching instant. In the meantime, the leakage inductance current and the gate-source voltage oscillations are also induced by the ZVS failure as shown in Fig. 14(b).

V. Conclusions

By taking into account the non-linear parasitic output capacitance of the power semiconductor devices, a voltage-based ZVS condition is proposed in this paper. Compared to the commonly used current- and energy-based methods, the voltage-based method is developed according to the practical transient switching procedure and thus it has a higher accuracy. Depending on the C_{oss} profile, which changes a lot with the drain-source voltage, the minimum leakage inductance currents can be obtained to achieve ZVS. Based on the practical results, the converter operating points are divided into three regions, i.e. safe ZVS region (total ZVS), marginal ZVS region (quasi-ZVS) and dangerous region (ZVS failure). Besides, a comparative analysis of the three methods is implemented by

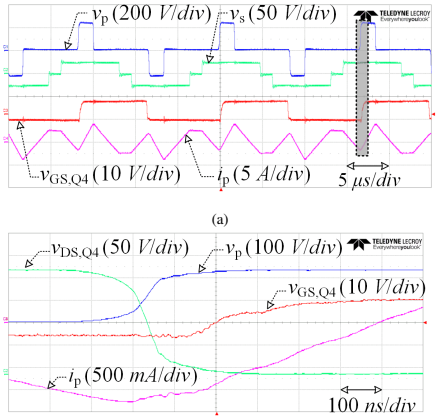


Fig. 12. Test point 1 (TP1, cf. black point in Fig. 11): steady state working waveforms within the safe ZVS region.

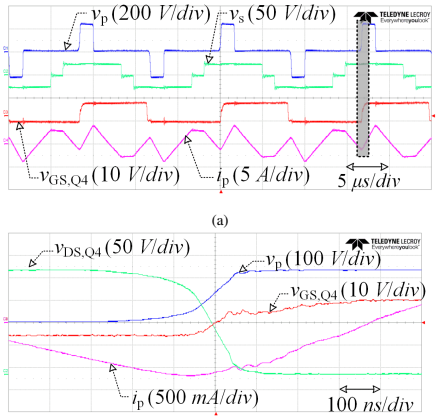
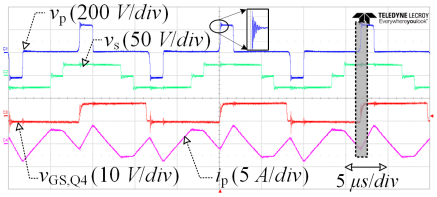


Fig. 13. Test point 2 (TP2, cf. blue point in Fig. 11): steady state working waveforms within the marginal ZVS region.

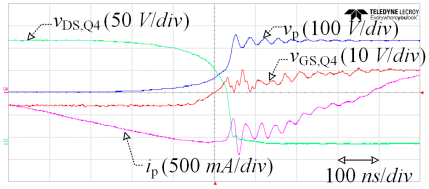
By taking into account the non-linear parasitic output capacitance of the power semiconductor devices, a voltage-based ZVS condition is proposed in this paper. Compared to the commonly used current- and energy-based methods, the voltage-based method is developed according to the practical transient switching procedure and thus it has a higher accuracy. Depending on the C_{oss} profile, which changes a lot with the drain-source voltage, the minimum leakage inductance currents can be obtained to achieve ZVS. Based on the practical results, the converter operating points are divided into three regions, i.e. safe ZVS region (total ZVS), marginal ZVS region (quasi-ZVS) and dangerous region (ZVS failure). Besides, a comparative analysis of the three methods is implemented by taking a triple-phase-shift operation mode as an example, and the same procedure can also be applied to other operation modes. In order for an effective validation, experimental results with different system specifications are conducted and the results can prove the effectiveness of the proposed voltage-based method by deriving a more accurate ZVS condition.

References

[1] R. D. Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high power density DC/DC converter for high power applica-



(a)



(b)

Fig. 14. Test point 3 (TP3, cf. red point in Fig. 11): Steady state working waveforms in the dangerous region.

tions," in *Conference Record of the 1988 IEEE Industry Applications Society Annual Meeting*, IEEE, 1988.

[2] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC–DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, 2012.

[3] S. Inoue and H. Akagi, "A bidirectional DC–DC converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, 2007.

[4] Z. Wang, B. Liu, L. Guan, Y. Zhang, M. Cheng, B. Zhang, and L. Xu, "A dual-channel magnetically integrated EV chargers based on double-stator-winding permanent-magnet synchronous machines," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1941–1953, Mar. 2019.

[5] Z. Qin, Y. Shen, P. C. Loh, H. Wang, and F. Blaabjerg, "A dual active bridge converter with an extended high-efficiency range by DC blocking capacitor voltage control," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5949–5966, Jul. 2018.

[6] A. Kadavelugu and S. Bhattacharya, "Design considerations and development of gate driver for 15 kV SiC IGBT," in *Proc. IEEE Applied Power Electronics Conf. and Exposition*, Mar. 2014, pp. 1494–1501.

[7] F. Z. Peng, and J. S. Lawler, "A new ZVS bidirectional DC-dc converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[8] B. Liu, Z. Wang, Y. Zhang, M. Cheng, and L. Xu, "The dual-channel magnetically integrated chargers for plug-in electric vehicles," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–7.

[9] Z. Wang, B. Liu, Y. Zhang, M. Cheng, K. Chu, and L. Xu, "The chaotic-based control of three-port isolated bidirectional dc/dc converters for electric and hybrid vehicles," *Energies*, vol. 9, no. 2, p. 83, 2016.

[10] B. Liu, P. Davari, and F. Blaabjerg, "A flexible control scheme for single-stage DAB AC/DC converters," in *Proc. IEEE Int. Power Electronics and Application Conf. and Exposition (PEAC)*, Nov. 2018, pp. 1–6.

[11] G. Oggier, G. O. García, and A. R. Oliva, "Modulation strategy to operate the dual active bridge DC-dc converter under soft switching in the whole operating range," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1228–1236, Apr. 2011.

[12] S. S. Shah, V. M. Iyer, and S. Bhattacharya, "Exact solution of ZVS boundaries and AC-port currents in dual active bridge type DC–dc converters," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5043–5047, Jun. 2019.

[13] B. Liu, P. Davari, and F. Blaabjerg, "An optimized control scheme to reduce the backflow power and peak current in dual active bridge converters," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, 2019, pp. 1622–1628.

[14] B. Liu, P. Davari, and F. Blaabjerg, "An optimized control scheme for reducing conduction and switching losses in dual active bridge converters," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 622–629.

[15] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando, and J. Sebastián, "Different purpose design strategies and techniques to improve the performance of a dual active bridge with phase-shift control," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 790–804, Feb. 2015.

Conference publication 4

An Enhanced Generalized Average Modeling of Dual Active Bridge Converters [C4]

B. Liu, P. Davari and F. Blaabjerg

The paper has been published in the
Proc. IEEE APEC, Mar. 2020, DOI: 10.1109/APEC39645.2020.9124001.

The layout has been revised.

An Enhanced Generalized Average Modeling of Dual Active Bridge Converters

Bochen Liu, Pooya Davari, Frede Blaabjerg
Department of Energy Technology
Aalborg University
Aalborg, Denmark
bli@et.aau.dk, pda@et.aau.dk, fbl@et.aau.dk

***Abstract*— An enhanced generalized average modeling (GAM) method for a dual active bridge (DAB) converter is presented in this paper. Firstly, the conventional lossless model is introduced and it is shown that this model might cause a non-neglectable steady state error. In order to improve the modeling accuracy, a wide range of loss sources are involved in the proposed enhanced GAM model, such as conduction losses and core losses. On this basis, this paper further proves that the 3^{rd}-order harmonic component of the leakage inductance current should be considered to reduce steady state errors in light load conditions, while others might only consider the 1^{st}-order harmonic in the existing DAB models. Also, a universal form of the modeling equation to include up to any h^{th}-order harmonic component is derived. Finally, comparative simulation and experimental results are presented to validate the feasibility of the analysis.**

***Keywords*—generalized average modeling, dual active bridge**

I. Introduction

The dual active bridge (DAB) dc-dc converter has been widely used in many applications such as distributed power systems and energy storage systems [1]–[5] due to its capabilities of matching different voltage levels and providing isolated and bidirectional power transfer. Besides, the inherent nature of zero voltage switching (ZVS) realization and simple symmetrical structure makes the DAB a potential candidate for high power density and modular applications [6], [7].

Many discrete-time models [8]–[11] of the DAB converter have been proposed to describe the converter states during different subintervals in one switching period and because of this, exact solutions for the studied state variables can be obtained. Even so, a continuous-time model is still worth researching since it can facilitate the controller design and provide an easy way to evaluate the whole system performance, especially when the DAB converter is used for modular system design.

Commonly, conventional averaging technique [12] extensively has been employed for power converter modeling. However, it requires a negligible current ripple, which is not applicable in DAB converters due to the ac transformer current. A generalized average model (GAM) [13] expands the state variables into Fourier series terms and provides a more clear representation of ac variables. Some papers [14], [15] have applied GAM to the DAB converter with focus on the tradeoff between accuracy and complexity. Of course, other methods can also be used to model the DAB converter, such as the time-domain analytical expressions based averaged modeling presented in [16], [17] and the discrete-time models [8], [10], [11], [18]. Among the previous works, the DAB is often taken as a lossless converter or only partial losses (e.g conduction losses) are taken into account, which will result in considerable steady state errors. Another problem is that usually only the 1^{st}-order term of the ac current is involved in the model, and this will also lead to errors especially in light load situations. On the other hand, for the time-domain analytical solution, a large amount of calculation is needed for solving the piecewise expressions in different sub-intervals, and this may become very complicated when more losses are considered.

In order to reduce the steady state error and unify the modeling procedure, an enhanced GAM for the DAB converter is presented in this paper. Various loss sources are considered in the enhanced GAM, including the conduction losses distributed on the on-state power devices, the isolating transformer and the auxiliary inductor, the core losses within the transformer and the losses from the equivalent series resistor in the DC capacitors. Besides, a universal modeling equation is derived to include up to k^{th}-order harmonic components of the leakage inductance current. For the remaining parts of this paper, the basic lossless model is firstly introduced, followed by an improved model considering power losses. In the lossy model, the steady state errors are calculated by only considering the 1^{st}-order harmonic of the leakage inductance current, and then in order to reduce the errors in light load, the model is further improved by considering the 3^{rd}-order harmonic component. Next, the experimental results are shown and the conclusions are summarized in the end.

II. Basic Model

The commonly used lossless model of the DAB converter can be simplified as shown in Fig. 1. V_{in} is the input DC voltage, and v_p, v_s are the terminal voltages of the primary H-bridge HB_1 and secondary H-bridge HB_2, respectively. i_L is the current flowing through the leakage inductance L, which is referred to the primary side of the transformer. i_o and v_o are the output current and the output DC voltage across the resistive load R_{load}.

The single phase shift modulation is applied to the DAB converter, and the working waveforms in one switching period are shown in Fig. 1(a). φ is phase shift angle between

978-1-7281-4829-8/20/$31.00 ©2020 IEEE

the voltages v_p and v_s. The diagonal power semiconductor devices in one H-bridge (e.g. S_1, S_4 in HB_1 in Fig. 1) are synchronously switched. If two switching functions $u_1(t)$ and $u_2(t)$ are introduced to HB_1 and HB_2, respectively, the following equations are satisfied.

$$u_1(t) = \begin{cases} 1, t \in [t_0, t_2] \rightarrow S_1, S_4 \text{ on} \\ -1, t \in [t_2, t_4] \rightarrow S_2, S_3 \text{ on} \end{cases}$$
$$u_2(t) = \begin{cases} 1, t \in [t_1, t_3] \rightarrow S_5, S_8 \text{ on} \\ -1, t \in [t_0, t_1) \cup (t_3, t_4] \rightarrow S_6, S_7 \text{ on} \end{cases} \quad (1)$$

Then the voltages v_p and v_s can be expressed by $v_p(t) = u_1(t) \cdot V_{in}$ and $v_s(t) = u_2(t) \cdot v_o(t)$, respectively. The lossless switched model can thus be obtained.

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L} u_1(t) \cdot V_{in} - \dfrac{n}{L} u_2(t) \cdot v_o(t) \\ \dfrac{dv_c(t)}{dt} = \dfrac{n}{C_o} u_2(t) \cdot i_L(t) - \dfrac{1}{R_{load} C_o} v_o(t) \end{cases} \quad (2)$$

For the convenience of derivation, $i_L(t)$, $v_o(t)$, $u_1(t)$, $u_2(t)$ in (2) are simplified with i_L, v_o, u_1, u_2, respectively. Focusing on the 1^{st}-order harmonic component of the high-frequency ac current i_L and the zeroth of the output DC voltage v_o, the generalized averaged model (GAM) can be derived from (2), resulting in

$$\begin{cases} \dfrac{d\langle i_L \rangle_1}{dt} = -j\omega \langle i_L \rangle_1 + \dfrac{1}{L} \langle u_1 \rangle_1 \cdot V_{in} - \dfrac{n}{L} \langle u_2 \cdot v_o \rangle_1 \\ \dfrac{d\langle v_o \rangle_0}{dt} = \dfrac{n}{C_o} \langle u_2 \cdot i_L \rangle_0 - \dfrac{1}{R_{load} C_o} \langle v_o \rangle_0 \end{cases} \quad (3)$$

where $\omega = 2\pi f_{sw}$ (f_{sw} is the switching frequency). In order to avoid transformer saturation, the dc components of the switching functions should be zero, namely $\langle u_1 \rangle_0 = \langle u_2 \rangle_0 = 0$. Therefore, according to [13], [19], there are

$$\begin{cases} \langle u_2 \cdot v_o \rangle_1 = \langle u_2 \rangle_1 \cdot \langle v_o \rangle_0 \\ \langle u_2 \cdot i_L \rangle_0 = \langle u_2 \rangle_1 \cdot \langle i_L \rangle_{-1} + \langle u_2 \rangle_{-1} \cdot \langle i_L \rangle_1 \end{cases} \quad (4)$$

Based on (1), the 1^{st}-order component of $u_1(t)$ and $u_2(t)$ can be calculated as

$$\langle u_1 \rangle_1 = \frac{2}{j\pi}, \quad \langle u_2 \rangle_1 = \frac{2}{j\pi} \cdot e^{-j\varphi} \quad (5)$$

Besides, for a periodic state variable x, the following relationships between the real (denoted by "R") and imaginary (denoted by "I") parts of $\langle x \rangle_k$ and $\langle x \rangle_{-k}$ are satisfied for the arbitrary k^{th} order coefficient.

$$\begin{cases} \langle x \rangle_{kR} = \dfrac{1}{T} \int_{t-T}^{T} x(\tau) cos(k\omega\tau) d\tau = \langle x \rangle_{-kR} \\ \langle x \rangle_{kI} = \dfrac{1}{T} \int_{t-T}^{T} x(\tau) sin(k\omega\tau) d\tau = -\langle x \rangle_{-kI} \end{cases} \quad (6)$$

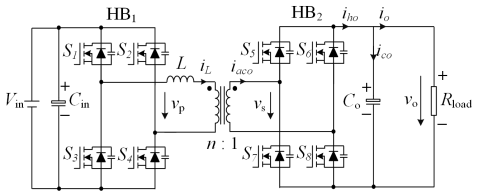


Fig. 1. Lossless DAB converter model with a resistive load.

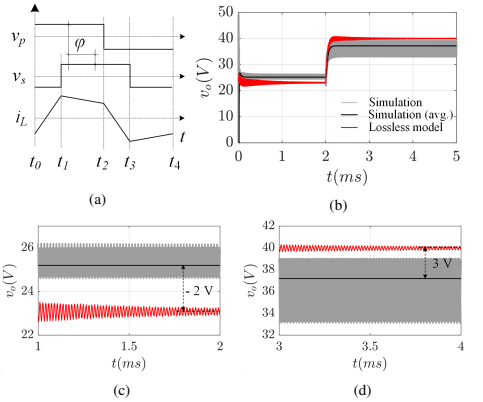


Fig. 2. Operating waveforms of the DAB converter (a) Typical working waveforms using single phase shift modulation. (b) Simulated and modeled step response by changing φ from 30^o to 60^o at t=2 ms, where the gray area is simulated v_o with switching ripples, the black solid line is the DC averaged value of the simulation results and the red is derived from (7). The corresponding simulation parameters are the same as the experiments, as listed in Table I. (c) Zoomed area from 1 ms to 2ms in Fig. 2(b). (d) Zoomed area from 3 ms to 4 ms in Fig. 2(b).

On the basis of (4) $\sim$ (6), the original GAM model in (3) can be transferred to a state-space form as

$$\frac{d}{dt} \begin{bmatrix} \langle i_L \rangle_{1R} \\ \langle i_L \rangle_{1I} \\ \langle v_o \rangle_0 \end{bmatrix} = \begin{bmatrix} 0 \\ -\dfrac{2}{\pi L} \\ 0 \end{bmatrix} V_{in} + \begin{bmatrix} 0 & \omega & \dfrac{2n}{\pi L} sin\varphi \\ -\omega & 0 & \dfrac{2n}{\pi L} cos\varphi \\ -\dfrac{4n}{\pi C_o} sin\varphi & -\dfrac{4n}{\pi C_o} cos\varphi & -\dfrac{1}{R_{load} C_o} \end{bmatrix} \begin{bmatrix} \langle i_L \rangle_{1R} \\ \langle i_L \rangle_{1I} \\ \langle v_o \rangle_0 \end{bmatrix} \quad (7)$$

and this is the lossless generalized average model of the DAB converter, which can be directly used for parameter estimation.

In order to evaluate the accuracy of (7), a step change of the phase shift φ (swiched from 30° to 60° at $t = 2\ ms$) is conducted, and the resultant voltage v_o responses from the simulation and (7) are shown in Fig. 2(b). The gray area is the simulated output voltage v_o with ripples, and the solid black line is the averaged value of v_o. The solid red lines are derived from (7), which have an obvious error from the

simulated average value in both light load ($\varphi = 30°$) and heavy load ($\varphi = 60°$) conditions.

In order to have a clear view of the voltage errors, the waveforms during $t \in [1\ ms,\ 2\ ms]$ and $t \in [3\ ms,\ 4\ ms]$ are amplified in Fig. 2(c) and Fig. 2(d), respectively. It can be seen that there exist non-negligible errors (denoted by ΔV_{err}) between the modeling and simulated results in either light load ($\varphi = 30°$, ΔV_{err} = -2 V) or heavy load ($\varphi = 60°$, ΔV_{err} = 3 V). Besides, the simulated average output voltages are around 23 V and 37 V in light and heavy load, respectively, and thus the voltage error percentages in two load situations can be calculated, which are both around 8%.

III. Enhanced GAM

As mentioned before, the commonly used lossless model is not accurate enough for estimating the output voltage in the real situation. In light of this, a new converter model considering the conduction losses, the core losses and the equivalent series resistor (ESR) of the output capacitor is built, as shown in Fig. 3(a). In the figure, the equivalent resistor R_{eq} referred to the primary side of the transformer (the turns ratio from primary to secondary side is $n:1$) is equal to

$$R_{eq} = 2R_{DS,onP} + R_{ind} + R_{trp} + n^2 R_{trs} + n^2 R_{DS,onS} \quad (8)$$

where $R_{DS,onP}$, $R_{DS,onS}$ are the on-state resistance of each primary and secondary transistor, and R_{ind}, R_{trp}, R_{trs} are the resistance of the auxiliary inductor, the primary winding and the secondary winding of the transformer, respectively. Due to that each switch of the secondary HB_2 is composed of two paralleled transistors for reducing the current stress, the referred on-state resistance is $n^2 R_{DS,onS}$ in (8). Besides, L_M in Fig. 3(a) is the magnetic inductance and R_M is used to symbolize the core losses.

Applying a similar derivation procedure as in lossless modeling, the lossy switched model can be obtained with (9) according to the lossy converter model in Fig. 3(a).

$$\begin{cases} \dfrac{di_{LM}}{dt} = \dfrac{n}{L_M} \cdot u_2 v_o \\ i_{RM} = \dfrac{n u_2 v_o}{R_M} \\ i_{ho} = n u_2 \cdot (i_L - i_{RM} - i_{LM}) \\ v_o = v_{co} + R_{ESR} \cdot C_o \dfrac{dv_{co}}{dt} \\ \dfrac{dv_{co}}{dt} = \dfrac{i_{ho}}{C_o} - \dfrac{v_o}{R_{load} C_o} \\ \dfrac{di_L}{dt} = -\dfrac{R_{eq}}{L} \cdot i_L + \dfrac{1}{L} \cdot u_1 V_{in} - \dfrac{n}{L} \cdot u_2 v_o \end{cases} \quad (9)$$

From the point of unifying the i_L analysis in GAM framework, it is worth to derive a universal equation including up to the h^{th} order components. By selecting the currents flowing in the leakage inductance (i_L), magnetic inductance (i_{LM}) and the voltages across the output capacitor (v_{co}), the resistive load (v_o) as the state variables, the universal GAM equation for modeling the lossy converter can be derived in (10). Therein, the k^{th} ($k = 1, 3, 5...h$) order component of i_L can be modeled by the first state-space expression, and since the magnetic current is usually much smaller than i_L, only the

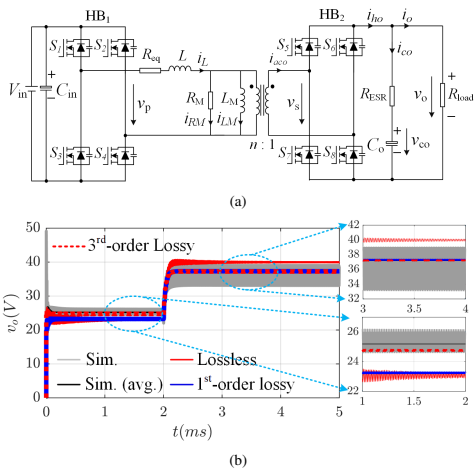


Fig. 3. Operating of the lossy DAB coverter (a) Lossy DAB converter model. (b) Simulated and modeled step responses by changing φ from 30^o to 60^o at $t = 2\ ms$, where the gray area, the black line, the solid red line are the same as shown in Fig. 1. The blue line and the dashed red line are derived from the lossy model in (10) with $h = 1$ ($k = 1$) and $h = 3$ ($k = 1, 3$), respectively.

1^{st} order component of i_{LM} is considered, as shown by the second state-space equation. On the DAB output side, unlike the lossless converter model, the capacitor voltage v_{co} is not equal to v_o any more and the relationships between them in the GAM framework can be expressed by the last two equations in (10). The symbol C_{sys} is a coefficient of the last equation and it is constant if a DAB setup is given.

For a comparative analysis, if h in (10) is set to be 1, the 1^{st}-order lossy model can be obtained, and the resulting step response is plotted by the blue curve in Fig. 3(b). Compared to the lossless response (solid red), the 1^{st}-order lossy model (blue) results in a much smaller error from the DC averaged curve (black) in the heavy-load situation ($\varphi = 60°$), as shown by the top-right inset in Fig. 3(b). Nevertheless, seen from the amplified bottom-right inset in Fig. 3(b), the resulting errors (blue) in light load ($\varphi = 30°$) are almost the same as the 1^{st}-order lossless model (solid red), both having a large error from the averaged value of the output voltage (black).

This phenomenon can be explained by the following: Assuming V_{p1}/V_{s1}, V_{p3}/V_{s3} are the peak value of the 1^{st} and 3^{rd} order components of the primary and secondary voltage v_p/v_s, the transferred power through the 1^{st} and 3^{rd} order components can be approximately calculated by P_{o1} and P_{o3}, respectively, which are

$$P_{o1} = V_{p1} V_{s1} \frac{sin\varphi}{\omega L}, \quad P_{o3} = V_{p3} V_{s3} \frac{|sin(3\varphi)|}{3\omega L} \quad (11)$$

Considering that $V_{p3} = 1/3 V_{p1}$ and $V_{s3} = 1/3 V_{s1}$, the ratio of P_{o3}/P_{o1} will be

$$\frac{P_{o3}}{P_{o1}} = \frac{sin(3\varphi)}{27 \cdot sin\varphi} \quad (12)$$

Based on (12), the relationship curve between the power ration P_{o3}/P_{o1} and the phase shift φ is shown in Fig. 4. If the converter works in heavy load, taking $\varphi = 70^\circ$ as an example, the resulting ratio is 2%, which can be neglected and it indicates that the 1^{st}-order modeling is accurate enough for heavy load situations (for the $\varphi = 60^\circ$ in Fig. 3(b) and the ratio P_{o3}/P_{o1} even becomes zero). However, in light load situations, the ratio sharply increases to 7.4% with $\varphi = 30^\circ$. Furthermore, if φ continually decreases so that $sin\varphi \approx \varphi$ and $sin(3\varphi) \approx 3\varphi$ are satisfied, the maximum P_{o3}/P_{o1} will reach 11%. In this case, the 3^{rd}-order component can not be neglected, and this also is the reason why the 1^{st}-order lossy modeling in Fig. 3(b) can help improve the heavy load performance, but has little effect in the light load.

In order to verify the theoretical analysis above, the modeled 3^{rd}-order response is also depicted by the dashed red line in Fig. 3(b), which is obtained with h = 3 in (10). It can be seen from the two right insets in Fig. 3(b) that compared to the lossless model (solid red) and the 1^{st}-order lossy model (blue), the 3^{rd}-order model can achieve much smaller errors in both light-load and heavy-load situations. Especially, the error between the 3^{rd}-order lossy model (blue) and the averaged simulation results (black) in light load is considerably reduced.

IV. Experimental Validation

A test platform shown in Fig. 5 is built. The converter parameters are listed in Table I, where T_{dead} is the dead time for the two transistors in the same leg and the subscripts "ind", "trp", "trs" denote the auxiliary inductor, the primary and secondary winding of the transformer, respectively. The leakage inductance referred to the primary side can be calculated by $L = L_{ind} + L_{trp} + n^2 L_{trs}$. Besides, the measured (or obtained from the data sheet) parameters of the passive components and the power devices are listed in Table II.

The step responses by switching the phase shift φ between 30° and 60° are illustrated in Fig. 6, including the step-up response in Fig. 6(a) and the step-down response in Fig. 6(b). Therein, v_o is the output voltage across the resistor load, v_p is the terminal voltage of the primary H-bridge and i_L is the leakage inductance current. In the step-up response, the steady

TABLE I
System Specifications

Parameters	Description	Value
P	Rating power	1.5 kW
V_{in}	Input DC voltage	120 V
$n:1$	Turns ratio of the transformer	3.5 : 1
f_{sw}	Switching frequency	60 kHz
T_{dead}	Dead time	400 ns
L_{ind}	Auxiliary inductor	36.2 μH
L_{trp}	Primary-side leakage inductance	4.5 μH
L_{trs}	Secondary-side leakage inductance	372.5 nH

TABLE II
Component Parameters of the Implemented Prototype

Components	Parameters
Auxiliary inductor: 10 turns Litz wire, 20 strands, 0.355 mm	R_{ind}= 27.9 mΩ @T_a= 25 ^oC
Primary winding of the DAB HF transformer: 35 turns copper foil	R_{trp}= 607.9 mΩ @T_a= 25 ^oC
Secondary winding of the DAB HF transformer: 10 turns copper foil	R_{trs}= 16.5 mΩ @T_a= 25 ^oC
Magnetic inductance of the transformer	L_M = 1.4 mH
Core losses resistance	R_M= 2kΩ @T_a= 25 ^oC
MOSFETs $S_1 \sim S_4$: IPW65R080CFD	$R_{DS,onp}$= 72 mΩ @T_j= 25 ^oC
MOSFETs $S_5 \sim S_8$: 2 x IPP110N20N3 in parallel	$R_{DS,ons}$=9.6 mΩ @T_j= 25 ^oC
Resistive load	R_{load}= 2.3 Ω
Output capacitor C_o: 2 x EETEE2D301HJ in parallel	R_{ESR}= 30 mΩ @T_a= 25 ^oC

$$
\begin{cases}
\dfrac{d}{dt}\begin{bmatrix}\langle i_L\rangle_{kR}\\ \langle i_L\rangle_{kI}\\ \langle v_o\rangle_0\end{bmatrix} = \begin{bmatrix}-R_{eq}/L & k\omega & \dfrac{2n}{k\pi L}sin(k\varphi)\\ -k\omega & -R_{eq}/L & \dfrac{2n}{k\pi L}cos(k\varphi)\\ 0 & 0 & 1\end{bmatrix}\times\begin{bmatrix}\langle i_L\rangle_{kR}\\ \langle i_L\rangle_{kI}\\ \langle v_o\rangle_0\end{bmatrix} + \begin{bmatrix}0\\ -\dfrac{2}{k\pi L}\\ 0\end{bmatrix}V_{in}\\
\dfrac{d}{dt}\begin{bmatrix}\langle i_{LM}\rangle_{1R}\\ \langle i_{LM}\rangle_{1I}\\ \langle v_o\rangle_0\end{bmatrix} = \begin{bmatrix}0 & \omega & -\dfrac{2n}{\pi L_M}sin\varphi\\ -\omega & 0 & -\dfrac{2n}{\pi L_M}cos\varphi\\ 0 & 0 & 1\end{bmatrix}\times\begin{bmatrix}\langle i_{LM}\rangle_{1R}\\ \langle i_{LM}\rangle_{1I}\\ \langle v_o\rangle_0\end{bmatrix}\\
\langle v_o\rangle_0 = \langle v_{co}\rangle_0 + R_{ESR}\cdot C_o\dfrac{d}{dt}\langle v_{co}\rangle_0,\quad C_{sys} = \dfrac{R_M R_{load}}{(n^2R_{ESR}+R_M)R_{load}+R_M R_{ESR}}\\
\dfrac{d}{dt}\langle v_{co}\rangle_0 = \dfrac{C_{sys}}{C_o}\left[\dfrac{-4n}{\pi}\sum_{k=1,3,5..}^{h}\dfrac{\langle i_L\rangle_{kR}sin(k\varphi)+\langle i_L\rangle_{kI}cos(k\varphi)}{k}+\right.\\
\qquad\left.\dfrac{4n}{\pi}\left(\langle i_{LM}\rangle_{1R}sin\varphi+\langle i_{LM}\rangle_{1I}cos\varphi\right)-\left(\dfrac{n^2}{R_M}+\dfrac{1}{R_{load}}\right)\langle v_{co}\rangle_0\right]
\end{cases}
\tag{10}
$$

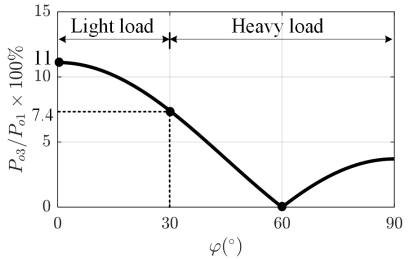


Fig. 4. Varying power ratios of the transferred power through the 3^{rd}-order component and the 1^{st}-order component of the leakage inductance current.

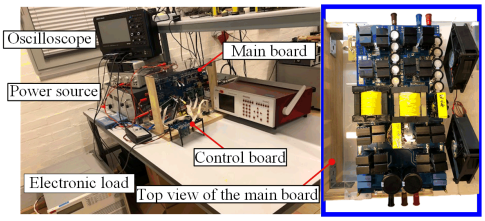


Fig. 5. Test platform for the DAB converter.

state working waveforms (as enclosed by the gray areas in Fig. 6(a)) are zoomed in Fig. 7, where v_s is the terminal voltage of the secondary H-bridge. Compared to the light load situation in Fig. 7(a), the output voltage becomes higher in Fig. 7(b) with an increased phase shift $\varphi = 60°$, leading to a different shape of the leakage inductance current i_p.

In order to evaluate the modeling accuracy, the waveform data of v_o from the oscilloscope is imported to MATLAB and averaged to compare with different modeling results, as shown in Fig. 8(a). Obviously, the lossless model (denoted by the solid red line) will cause large errors from the averaged output voltage (denoted by the solid black line) in both load situations.

In order for a better view to compare the 1^{st}-order model and the 3^{rd}-order model, the waveforms within $[0.02s, 0.04s]$ and $[-0.03s, -0.01s]$ are amplified in Fig. 8(b) and Fig. 8(c), corresponding to the heavy load and light load, respectively. Seen from Fig. 8(b), the modeling results from the 1^{st}-order lossy model (denoted by the solid blue line) and the 3^{rd}-order lossy model (denoted by the dashed red line) are almost overlapped, and both achieve a more accurate result than the lossless model. Nevertheless, the 3^{rd}-order model also can considerably improve the modeling accuracy in light load situations, where the 1^{st}-order model has little effect and appears close to the lossless model in Fig. 8(c). These results indicate that the lossy GAM model including the 1^{st} and 3^{rd} components has the smallest error in both light- and heavy-load situations, which agrees well with the analysis before and signifies the correctness of the improved modeling method.

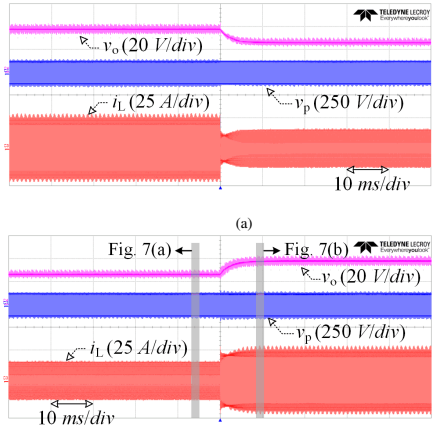


Fig. 6. Measured step response of the DAB converter: (a) with φ changing from 60° to 30°. (b) with φ changing from 30° to 60°.

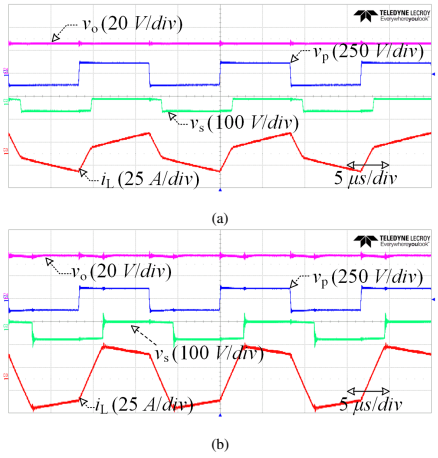
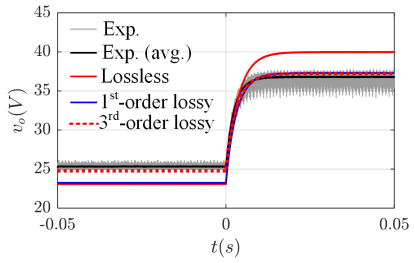


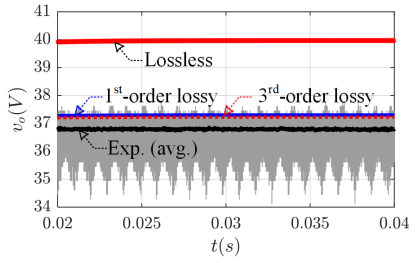
Fig. 7. Measure steady state operating waveforms of the DAB converter with (a) $\varphi = 30°$. (b) $\varphi = 60°$.

V. Conclusions

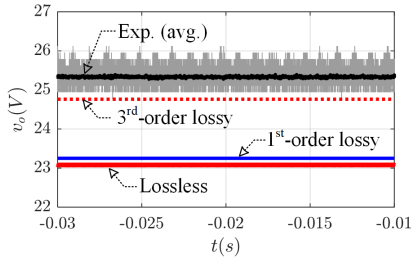
By involving an enhanced power loss consideration and the 3^{rd}-order component of the ac current, the improved GAM of the DAB converter can achieve a considerably reduced steady state error compared to the conventional lossless modeling or by only considering the 1^{st}-order term. Besides, the usage of the 3^{rd} harmonic is emphasized in light load situations, and furthermore, a universal generalized average modeling method can be achieved by adopting the derived unified k^{th}-order model in this paper. The feasibility of the modeling analysis



(a)



(b)



(c)

Fig. 8. Comparison of the experimental and the modeling results with a step response (a) phase shift φ changed from 30° to 60° at $t = 0s$. (b) Zoomed-in waveforms for $t \in [0.02s, 0.04s]$ in Fig. 8(a). (c)Zoomed-in waveforms for $t \in [-0.03s, -0.01s]$ in Fig. 8(a).

is validated with simulation and experimental results.

REFERENCES

[1] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC–DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, 2012.

[2] S. Inoue and H. Akagi, "A bidirectional DC–DC converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, 2007.

[3] B. Liu, P. Davari, and F. Blaabjerg, "A flexible control scheme for single-stage DAB AC/DC converters," in *Proc. IEEE Int. Power Electronics and Application Conf. and Exposition (PEAC)*, Nov. 2018, pp. 1–6.

[4] Z. Wang, B. Liu, L. Guan, Y. Zhang, M. Cheng, B. Zhang, and L. Xu, "A dual-channel magnetically integrated EV chargers based on double-stator-winding permanent-magnet synchronous machines," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1941–1953, Mar. 2019.

[5] Z. Wang, B. Liu, Y. Zhang, M. Cheng, K. Chu, and L. Xu, "The chaotic-based control of three-port isolated bidirectional dc/dc converters for electric and hybrid vehicles," *Energies*, vol. 9, no. 2, p. 83, 2016.

[6] B. Liu, P. Davari, and F. Blaabjerg, "An optimized control scheme for reducing conduction and switching losses in dual active bridge converters," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 622–629.

[7] B. Liu, P. Davari, and F. Blaabjerg, "An optimized control scheme to reduce the backflow power and peak current in dual active bridge converters," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, 2019, pp. 1622–1628.

[8] C. Zhao, S. D. Round, and J. W. Kolar, "Full-order averaging modelling of zero-voltage-switching phase-shift bidirectional DC-dc converters," *IET Power Electron.*, vol. 3, no. 3, pp. 400–410, May 2010.

[9] F. Krismer and J. W. Kolar, "Accurate small-signal model for an automotive bidirectional dual active bridge converter," in *Proc. 11th Workshop Control and Modeling for Power Electronics*, Aug. 2008, pp. 1–10.

[10] L. Shi, W. Lei, Z. Li, J. Huang, Y. Cui, and Y. Wang, "Bilinear discrete-time modeling and stability analysis of the digitally controlled dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8787–8799, Nov. 2017.

[11] D. Costinett, "Reduced order discrete time modeling of ZVS transition dynamics in the dual active bridge converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, Mar. 2015, pp. 365–370.

[12] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *Proc. IEEE Power Electronics Specialists Conference*, Jun. 1976, pp. 18–34.

[13] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 251–259, Apr. 1991.

[14] J. A. Mueller and J. W. Kimball, "An improved generalized average model of dc–dc dual active bridge converters," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9975–9988, Nov. 2018.

[15] H. Qin and J. W. Kimball, "Generalized average modeling of dual active bridge DC–dc converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2078–2084, Apr. 2012.

[16] K. Zhang, Z. Shan, and J. Jatskevich, "Large-and small-signal average-value modeling of dual-active-bridge dc–dc converter considering power losses," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1964–1974, Mar. 2016.

[17] H. Bai, C. Mi, C. Wang, and S. Gargies, "The dynamic model and hybrid phase-shift control of a dual-active-bridge converter," in *Proc. 34th Annual Conf. of IEEE Industrial Electronics*, Nov. 2008, pp. 2840–2845.

[18] F. Krismer and J. W. Kolar, "Accurate small-signal model for the digital control of an automotive bidirectional dual active bridge," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2756–2768, Dec. 2009.

[19] V. A. Caliskan, O. C. Verghese, and A. M. Stankovic, "Multifrequency averaging of DC/dc converters," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 124–133, Jan. 1999.

ISSN (online): 2446-1636
ISBN (online): 978-87-7210-807-0 AALBORG UNIVERSITY PRESS